

## Plasmonic technology innovation: The chip-to-chip interconnect

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**Abstract:** This report presents the innovation potential for chip-to-chip plasmonic interconnects and European-funded project NAVOLCHI that aims to fulfill the promise. Plasmonic interconnects are a special kind of optical interconnects, i.e. they utilize the superior bandwidth of light to achieve great speeds of data flow. Plasmonic interconnects may resolve known bottleneck issues in communications, such as the multi-core processor-to-memory bottleneck in the cell phone industry. In addition, the plasmonic elements of the interconnect can be extremely compact, thus bridging the size gap between electronics and silicon photonics. NAVOLCHI utilizes a CMOS-compatible approach that will ensure the cost-effectiveness of the future product.

NAVOLCHI, a European Union-funded project, explores, develops and aims to demonstrate a novel nano-scale plasmonic chip-to-chip and system-in-package (SiP) interconnect to overcome the bandwidth, footprint and power consumption limitations of today's electrical and optical interconnect solutions. Today, electronics is limited in operating speed, while photonics is limited in miniaturization capability. By use of the emerging science of

plasmonics, NAVOLCHI aims to bridge the gap between electronics and photonics, paving the way for the faster and smaller chip technology of the future.

The NAVOLCHI interconnect will comprise plasmonic transceivers: Key elements to be developed are plasmonic lasers and modulators for the transmitter, plasmonic amplifiers and detectors for the receiver. The plasmonic devices will be monolithically integrated on an industry-friendly CMOS platform.

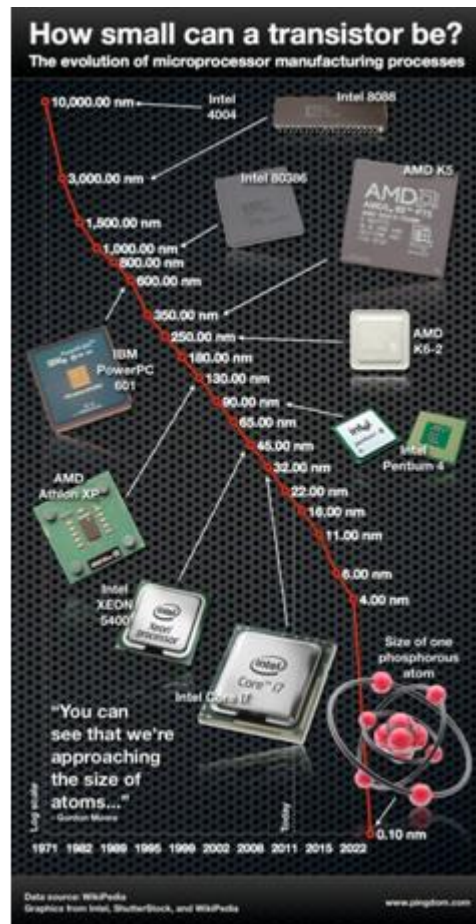


Figure 1: At the 22 nm node, transistor features are the size of tens of silicon lattice constants, and the near-future forecast involves integrated devices that consist of merely a few atoms. Thus, changes to technologies of choice are in order. Picture taken from [1].

devices that consist of merely a few atoms.

Performance scales favorably with increased integration and reduced size. Signal delay scales linearly with length, while power consumption follows a square law. However, as dimensions are reduced, parasitic capacitance increases and system delay becomes comparable to computation delays. In addition, the physical limit for miniaturization of this technology is approaching (see Fig. 1). The constant innovation on bandwidth-hungry user applications and the growing needs for computation power are bound to unveil further the limitations of electronics.

In the following sections, we will present the innovation potential in NAVOLCHI and plasmonics interconnects; we will review the limitations in speed and size of electronics, the bandwidth advantage that photonic devices enjoy over electronic ones. The size advantage of plasmonics over conventional photonics will be reviewed, establishing the promise of plasmonics for increased integration. The report will conclude by detailing how the NAVOLCHI project will utilize plasmonics in chip-to-chip interconnects in order to overcome the bandwidth, footprint, and power consumption challenges present in competing technologies.

## Electronics and limitations

Electronics has been following Moore's Law for more than five decades and the number of transistors on integrated circuits has been increasing at an exponential rate by doubling every 18 months. At the 22 nm node, transistor features are the size of tens of silicon lattice constants, and the forecast for the near future involves integrated

### Electronics and the cell phone industry

Today, the electronic systems market is mainly driven by the cellular phone industries where cost, size, performance and time to market are the primary driving forces. Cellular phone companies have been fighting for market share by increasing phone features through additional capabilities such as camera, FM radio, color screen, Bluetooth, Internet access, global positioning (GPS), video, sensors and other applications, requiring additional power in an ever shrinking form factor, volume and weight in order to decrease the average selling price.

Recent phone benchmarking studies showed that both Silicon integration and packaging technologies have driven the system miniaturization without increase in board routing complexity and with surprising low discrete component integration. The higher die area is actually due to increase functionalities and memory size.

Beyond the miniaturization trend, talk and standby times have been key selling points for cellular phone manufacturers, driving the pressure on IC suppliers to offer highly integrated but low-power consumption devices that do not strain handset battery lifetimes. Cellular phones are becoming increasingly small, dense and power-hungry, offsetting the size and energy density advances offered by the lithium-ion battery sources powering them.

In short, battery development has not kept pace with Moore's law and its subsequent power demands. As new applications and services become available, it is anticipated that the computing power available to incorporate into mobile devices will always be limited by finite power sources. As a consequence, mobile phone board designers are looking for every opportunity to save every milliamp of current in order to extend battery life as much as possible.

Another aspect to take into account is that both communications and digital IC technologies are moving progressively towards higher frequencies, such that the limiting factor for many wireless components is often the package parasitic effects, not the IC itself. Packaging parasitic factors can limit the frequency response or signal integrity of an otherwise robust design, preventing it from reaching its operation speed potential. Reducing inductance and capacitance of interconnections would help reduce time delays and improve electrical performance. Dielectric technology must then be chosen to ensure both low dielectric constant and low dielectric loss.

Today, cellular phones are by far the largest market for Systems in Package (SiP). Multi-Chip Modules and SiP introduce a different kind of issue: the issue of chip-to-chip communication. In multi-processor systems the memory chip needs to communicate with all processors at the same time, and this communication channel becomes the data rate bottleneck (see Fig. 2). In addition, while the number of processors per system will continue to increase, the clock frequency will remain almost the same due to several thermal constraints [2]. Therefore, the overall performance of the multi-processor systems will depend on how efficiently interconnects are utilized for the communication requirements of

these systems. High performance interconnects of great bandwidth, reduced latency and low power consumption will be required in the future.

In this section, the limitations and challenges of electronics in today's chip market have been presented. Size and power issues, as well as data rate bottlenecks call for a different perspective. Here comes...

## **The optical interconnect**

A solution to the problem of chip-to-chip communication can be in the form of optical interconnects. Optical interconnects have significant advantages over electrical ones. Perhaps the most important advantage is that they present much superior bandwidth. In addition, they present the advantages of lower attenuation, minimum crosstalk among neighboring channels, lower jitter, lower dispersion, simple impedance matching, speed-of-light signal propagation, and minimization of the needs for high-power equalization and pre-emphasis [3, 4, 5]. Optical interconnect solutions used to focus only on limited opportunities in supercomputers and highest-end telecom. However, optical interconnects are now considered as the viable solution for high-power computing and data centres. A CIR report from 2010 [6] estimated that the market opportunity for optical interconnects will amount to \$3.5 billion by 2015 due to their cost-efficiency and capacity to confront the upcoming bandwidth challenges for interconnection more efficiently than copper wires. Chip-to-chip optical interconnects, in particular, are not expected to create revenue before 2018. This is due to the technological and cost challenges that need to be overcome. Even so, optical chip-to-chip interconnects are already considered as an enabling technology for computer and telecom equipment, because they are capable of increasing board-level communication speeds.

Optical fibers have the capacity of transmitting digital information more than 1000 times faster than electronics. However, fibers are bulky and are not appropriate for board-level communication. Silicon photonics is a technology that is being heavily invested in (see, e.g., [7]), so that the superior bandwidth capacity of light is brought to chip-scale level. Yet, conventional photonics is diffraction-limited: at best, signals can only be focused to a size that is on the order of magnitude of the wavelength (i.e. several hundreds of nanometers, i.e. one to two orders of magnitude larger than current electronics). New layers have to be added to hybrid electronic-photonics chips in order to overcome the size incompatibility, increasing complexity and cost. In view of the above, the challenge is to combine the best aspects of electronics and photonics, i.e. the miniaturization capability of electronics with the superior bandwidth and other advantages of photonics, in order to create the smaller, faster and energy efficient integrated chips of the future.

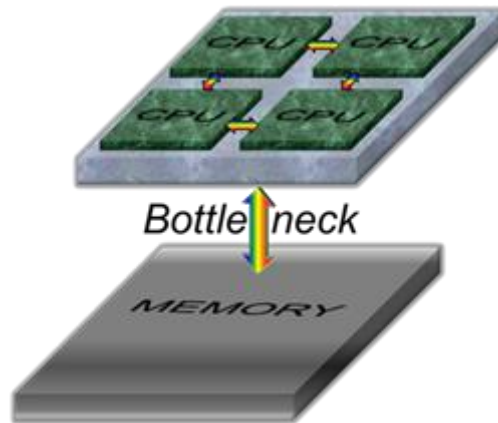


Figure 2: In multi-processor systems the memory chip needs to communicate with all processors at the same time, and this communication channel becomes the data rate bottleneck.

## Optical interconnect with plasmonic transceivers: The plasmonic interconnect

Plasmonics [8, 9] is a cutting-edge science that may bridge the electronics-photonics size gap while retaining the bandwidth and other advantages of silicon photonics. The carriers of information in plasmonic devices are Surface Plasmon-Polaritons (SPPs), electromagnetic fields that travel along the interfaces between metals and insulators and can be used to carry information at optical bandwidths. SPPs decay exponentially away from metal-insulator interfaces and are very compact in space. SPPs can beat the diffraction limit and can be manipulated in subwavelength scales, allowing for the design of subwavelength optical devices. The size gap between photonics and electronics can thereby be bridged in hybrid electronic-plasmonic chips, while the superior bandwidth capability of light is utilized. In addition, plasmonic devices involve the presence of metals and so do electrical circuits. In a hybrid electronic-plasmonic integrated circuit, the metals can be used to transmit both electric and optical signals, allowing for a very compact and efficient design.

Thus, plasmonic devices have the potential to utilize the advantages of photonics at the size-scale of electronics (see Fig. 3). This promise has attracted a lot of scientific interest for plasmonics in the past few years; but there are still many scientific and technological challenges to be overcome so that the promise is fulfilled.

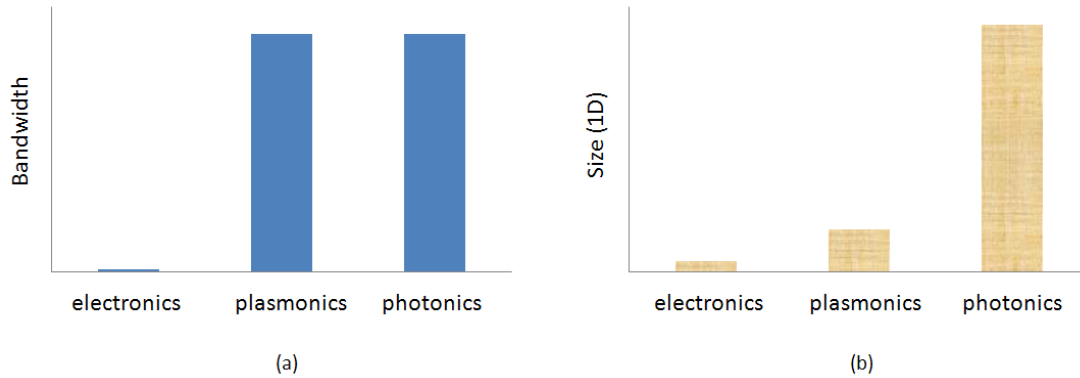


Figure 3: (a) Relative bandwidth comparison for various technologies. Plasmonics utilizes light as the carrier just as traditional photonics. Electronics is thus 1000 times slower. (b) Relative size comparison in one dimension. Electronics and plasmonics are on the order of tens of nanometers, while conventional photonics is diffraction-limited to hundreds of nanometers for telecom or visible operating wavelengths. In two dimensions (i.e. the surface area of an integrated chip), this relative size comparison follows a square law and the difference in size is bigger.

## The NAVOLCHI project and plasmonic interconnects

In November 2011, EU-funded project NAVOLCHI [10] set out to develop a CMOS-compatible chip-to-chip optical interconnect with plasmonic transceivers, i.e. a plasmonic interconnect (see Fig. 4). The aim is that the plasmonic interconnect will be of the smallest cost, power consumption and footprint with respect to competing technologies, and will lead high power computing and data centres to the Tbit/s era.

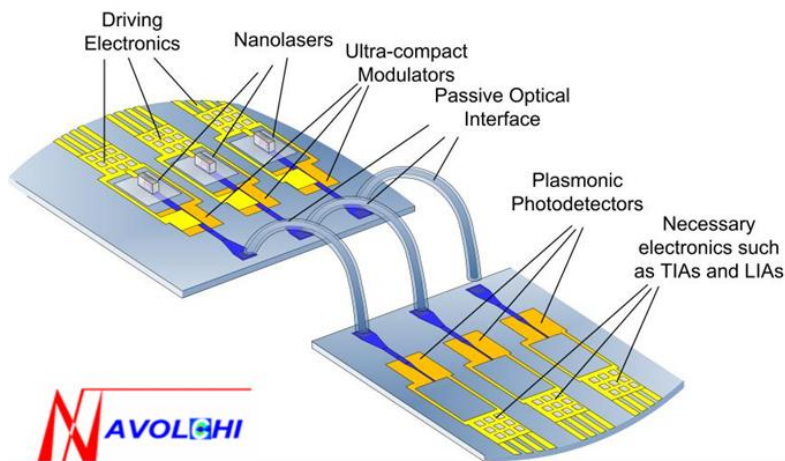


Figure 4: One of the schemes to be tested in NAVOLCHI for interconnection of 2 CMOS chips. The transceivers comprise plasmonic devices.

The plasmonic transceivers will consist of monolithically integrated metallic nanolasers and plasmonic modulators at the transmitter, and monolithically integrated plasmonic amplifiers and plasmonic detectors at the receiver, all on CMOS platform. The technology suggested in NAVOLCHI relies on standardized processes of the silicon industry and allows for massive monolithic integration with very low production cost.

There is high technological and innovation value not only in the final interconnect system that NAVOLCHI will present, but also in the device elements that the system comprises. These plasmonic elements add significant innovation value as stand-alone devices, as they may provide solutions to different applications (e.g. sensors, waveguiding, etc.). In particular, the subsystem devices that are going to be developed within NAVOLCHI are the following:

### **Metallic nanolaser**

In the metallic nanolaser, a metal cladding is used to shrink the optical lasing mode to the smallest possible size given by the diffraction limit. It promises room temperature operation with a current injection of only a few microamperes and will offer low power consumption as well as ultra-fast switching. Furthermore, the particular design of this device can be extended for use in other nanophotonic applications, such as metallic-coated semiconductor optical amplifiers, devices for digital signal processing and ultra-compact metallic laser arrays.

### **Plasmonic modulator**

The surface plasmon-polariton absorption modulator is shown to be promising for high speed and low power consumption switching [11, 12]. An extinction ratio of 20 dB has been demonstrated in a 5  $\mu\text{m}$ -long device for an applied DC voltage of 2.5 V [12]. The approach takes advantage of the strong optical field confinement in highly nonlinear indium tin oxide (ITO) layer [11]. Due to the high electron mobility in ITO, the device can operate in speeds up to 100GHz and beyond.

### **Plasmonic amplifier**

Since the transmitter is expected to deliver a low signal level, the first element in the receiver is a plasmonic amplifier able to provide a 10 dB gain at the operation wavelength. This operation is necessary to supply the appropriate power to be measured by the photodetector with a good signal to noise ratio. Such amplifier fulfills the requirements to be integrated in a silicon platform and operate under either optical or electrical pumping. For this purpose, technologies based on active polymer and colloidal quantum dots nanocomposites and SOI waveguides are being studied. The metals forming the plasmonic waveguides have a dual function. On the one hand they ensure high field confinement in the active layer. On the other hand they can also serve as the electrical contact to inject current into the gain layer. Beyond NAVOLCHI, this device can be used wherever an integrated amplifier is desired. In addition, by integrating the amplifier within an optical cavity, new types of lasers can be realized.

### **Plasmonic photodetector**

Once the plasmonic amplifier has provided a good signal level, the photodetector will convert incoming light into electrical information. In order to improve the responsivity and reduce chip dimensions, a plasmonic detector based on quantum dots and metal

nanostructures will be built. Hence semiconductor quantum dots should have good absorption properties at the operation wavelength. The role of metal nanostructures is to improve the signal by photon-plasmon interaction. Another possibility is the direct conversion of plasmon-polaritons (produced by incoming light at metal nanostructures) into electrons if they are embedded in conductive polymer.

## Conclusion

Silicon electronics has driven technological revolution in the past decades. However, we are reaching its fundamental limitations. Photonics utilizes light in order to connect systems and process information 1000 times faster than electronics. But traditional photonics cannot achieve the compactness needed for integrated circuits, as light is diffraction-limited to sizes that are 2 orders of magnitude larger than electronics.

We want to have the best of both worlds: The size of electronics and the bandwidth of photonics. Plasmonics is an emerging field that utilizes light as the information carrier in metal/dielectric structures. In such plasmonic structures, light is not diffraction-limited in size and subwavelength devices become possible, achieving the compactness of electronics. Thus, plasmonics promises to bridge the gap between electronics and photonics, offering great speeds at compact sizes for the integrated circuits of the future.

The NAVOLCHI project utilizes the plasmonics approach to combat an important contemporary problem in multi-core computing. NAVOLCHI aims to design and build a plasmonic chip-to-chip interconnect to resolve the data-rate bottleneck for the connection of multi-core chips to other chips. Using the industry-friendly CMOS platform, the goal is for the plasmonic chip-to-chip interconnect to offer great speeds at small size, and low power consumption at a very low cost. At the same time, NAVOLCHI will enable the members of its consortium to develop cutting-edge plasmonic subsystems that may also find application elsewhere.

NAVOLCHI finishes in October 2014.

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