



Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Second Intermediate Progress Report

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List of Partners concerned

Partner number	Partner name	Partner short name	Country	Date enter project	Date exit project
1	Karlsruher Institut für Technologie	KIT	Germany	M1	M36
2	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMEC	Belgium	M1	M36
3	TECHNISCHE UNIVERSITEIT EINDHOVEN	TU/e	Netherlands	M1	M36
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Executive Summary

This document shall incorporate (all) rules procedures concerning the technical and administrative management of the project and is therefore to be updated on a regular basis. Please look at www.navolchi.eu regularly for the latest version.

Change Records

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INTERMEDIATE PROGRESS REPORT 2

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² Usually the contact person of the coordinator as specified in Art. 8.1. of the Grant Agreement.

³ The home page of the website should contain the generic European flag and the FP7 logo which are available in electronic format at the Europa website (logo of the European flag: http://europa.eu/abc/symbols/emblem/index_en.htm logo of the 7th FP: http://ec.europa.eu/research/fp7/index_en.cfm?pg=logos). The area of activity of the project should also be mentioned.

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1 Introduction

The report here present summarizes the results and achievements during month 18 and month 27 of the NAVOLCHI project. It is the second intermediate report out of a list of four major reports during the project:

- First Intermediate Report after 9 months,
- First Periodic Activity Report after 18 months,
- Second Intermediate Report after 27 months and
- Second Periodic Activity Report after 36 months.

Additionally, a final report will follow in the end of the project.

Due to its 'intermediate' character, this report focuses mainly on the technological and scientific achievements along the report period. Although following the outline of a regular periodic report, some parts have been omitted or changed: Contrary to a periodic report, here the 'Declaration by the scientific representative of the project coordinator' is not needed and the 'Publishable summary' has changed to a simple 'Summary'. Additionally, no finances, no manpower and no FormCs are prepared, because this is necessary for the periodic and final reports only.

2 Summary

The Project

The NAVOLCHI project explores, develops and demonstrates a novel nano-scale plasmonic chip-to-chip and system-in-package interconnection platform to overcome the bandwidth, foot-print and power consumption limitations of today's electrical and optical interconnect solutions. The technology exploits the ultra-compact dimensions and fast electronic interaction times offered by surface plasmon polaritons to build plasmonic transceivers with a few square-micron footprints and speeds only limited by the RC constants. Key elements developed in this project are monolithically integrated plasmonic lasers, modulators, amplifiers and detectors on a CMOS platform. The transceivers will be interconnected by free space and fiber connect schemes. The plasmonic transceiver concept aims at overcoming the challenges posed by the need for massive parallel interchip communications. Yet, it is more fundamental as the availability of cheap miniaturized transmitters and detectors on a single chip will enable new applications in sensing, biomedical testing and many other fields where masses of lasers and detectors are needed to e.g. analyze samples. Economically, the suggested technology is a viable approach for a massive monolithic integration of optoelectronic functions on Si substrates as it relies to the most part on the standardized processes offered by the silicon industry. In addition, the design and production cost of plasmonic devices are extremely low and with the dimension 100 times smaller over conventional devices they will require much lower energy to transfer data over short ranges of multi-processor cluster systems. The project is disruptive and challenging, but it is clearly within the area of expertise of the consortium. It actually builds on the partners prior state of the art such as the demonstration of the first nano-scale plasmonic pillar laser. This project has the potential to create novel high-impact technologies by taking advantage of the manifold possibilities offered by plasmonic effects.

Project Status

During the time after the first periodic report in month 18 of the NAVOLCHI project, the development of the core components has been of major concern. The plasmonic devices are divided into

- the transmitter and
- the receiver, subdivided into the amplifier and the QD-photodetector.

While the analysis part and the definition part of the demonstrator device is handled in WP2, the WPs 3 and 4 deal with the core components. The realization of the optical and electrical interfaces for the plasmonic interconnection platform is focused in WP5. As core tasks in this project, these work packages 2-5 will be discussed in more detail.

According to plan, activities have been started in WP6, which handles characterization of the devices and system integration to a demonstrator device.

The project is accompanied by the management WP1 and by WP7, which cares for publication and dissemination work.

WP1 (Project Management) Summary

The consortium is working well together and the most important deliverables and milestones have been achieved during the last period. Major changes and future plans are listed below and discussed in detail within the particular sections.

- Since June 2013, Prof. Dr. Jürg Leuthold (KIT / ETH) acts as Technical Project Manager and Prof. Dr. Manfred Kohl (KIT) is Coordinator (see 3.3.1).
- ST intends to reduce its engagement in work package 6 (see 3.3.6).
- The Consortium intends to include ETH as an additional partner of the NAVOLCHI project, who should take over activities of work package 6 (see 3.3.6).
- The Consortium intends to extend the project activities by 6 month due to delays in development of fabrication technology and due to STs reduced engagement in WP6 (see 3.3.7).

In chapter 3.2.6 section ‘task 6.4’ (page 53) it is mentioned, that a detailed reply on the reviewers comments on the last review meeting after month 18 will be given in milestone MS39 following this report by end of May 2014.

WP2 (Interconnect Specifications) Summary

WP2 investigates the new plasmonic device technology for chip-to-chip interconnection. In the context of WP2, the requirements and needs for chip-to-chip interconnects have been reviewed. Initial benchmarking has been performed. In view of the benchmarking review, industrial partner’s ST input and all partner’s contributions, targeted specifications have been set for the system in order for the plasmonic interconnect to be competitive and, eventually, outperform competing technologies. A simulation platform has been implemented for the design space exploration and the extraction of the sub-system specifications. The simulation platform has been realized with the commercial VPI Photonics software. Eight different configurations have been studied in total: with direct or indirect modulation, with plasmonic or PIN detector, with or without amplifier. The Bit Error Rate has been calculated for each case, sweeping parameters such as the laser output power or the amplifier gain. The study is focused on the question of device characteristics, so that the system target specifications are achieved. The eight different configurations that have been studied is part of the design space exploration that has been performed in order to find the configuration that better meets the system requirements. The final definitions of the subsystem devices have been defined and the system design scenarios have been selected. Furthermore, the interfaces of the plasmonic modules have been defined and the required electronic systems for the transceivers have been implemented and evaluated.

WP3 (Plasmonic Transmitter) Summary

It is the aim of WP3 for the reporting period to carry out the fabrication of a plasmonic/metallic laser and a plasmonic modulator. The metallic laser is developed in a III-V wafer bonded to silicon, whereas the plasmonic modulator is developed on Silicon-on-insulator. Within such a period, key non-standard fabrication processes for the fabrication of the metallic nanolaser were developed. Furthermore, the first run of metallic lasers was carried out and a few problems were identified, which must be solved before lasing can be achieved. Two types of plasmonic modulators are fabricated on silicon-on-insulator wafers, namely the surface plasmon polariton absorption

modulator and the plasmonic phase modulator. Initial DC characterization of the absorption modulators show 6dB extinction ratio for a switching voltage of 3V. The fabricated plasmonic phase modulators exhibit flat RF frequency response up to 65 GHz. The useability of the modulator in a real 40Gbit/s system is validated. Milestones 14 and 15 have been reached within the reported period, as well as deliverables D3.3 and D3.4.

WP4 (Plasmonic Receiver) Summary

The fundamental properties of a novel QD material, HgTe, were characterised in depth using ultrafast absorption spectroscopy and nearly threshold-less gain was observed. From these measurements we could estimate a peak gain of at least 400 dB/cm for a closed-packed film of this material, indicating that the project target of reaching 10 dB gain under optical pumping should be within reach. The next step now is to demonstrate such gain also for QDs deposited on a substrate, either directly or dispersed into a suitable polymer. In parallel, the two concepts of hybrid-plasmonic amplifiers incorporating QDs (using polymer and SiN waveguides) have been fabricated and validated, waiting for optimized HgTe QDs; also metal waveguides (planar and ridges) have been fabricated and measured the propagation length of the surface plasmon polariton by using a new method.

In the case of photodetectors based on quantum dots important advances have been reached in the last months: i) conductive films based on PbS QDs absorbing at wavelengths shorter than 1700 nm were achieved, ii) measured responsivities in Schottky-heterostructure photodetectors were around 0.095 - 0.080 A/W in the range 1000 - 1500 nm. The QD-films were prepared by dr. blading that promoted an improvement of photodiode electrical (dark current reduction) and electro-optical (short circuit current and open circuit voltage under illumination) characteristics. The design of a new kind of plasmonic photoconductor was made by considering a plasmonic nano-gap waveguide concept; a first generation of these structures has been accomplished in collaboration with TUE-group and currently being processed at UVEG.

WP5 (Optical and Electrical Interfaces) Summary

WP5 focuses on realizing the optical and electrical interfaces for the plasmonic interconnection platform. KTH demonstrated an optimized version of the couplers between silicon and plasmonic waveguides. Through process and design improvements the losses are now below 1dB. In parallel also the simulation of a side coupler was carried out. IMEC carried out simulations and optimizations for a second generation beam coupler, aiming at coupling between two silicon photonics chips. Based on these simulations a mask is now being prepared. ST developed a new PHY adapter, and integrated it with the models developed in WP2. At the same time ST started implementation of the circuits in an FPGA.

WP6 (Integration, Characterising and Testing) Summary

Characterisation of active and passive plasmonic devices started at month 7.

WP7 (Exploitation and Dissemination) Summary

Dissemination and exploitation of ideas and results is of high importance in the project. There is substantial dissemination action concerning project activities. In particular, NAVOLCHI partners

have already produced **XXX** high quality scientific journal and **XXX** conference publications (papers/presentations/talks). The project website (www.navolchi.eu) has been implemented and uploaded online, disseminating the NAVOLCHI activities further. A press release and an advertising brochure have been issued.

On the exploitation front, 1 patent has been submitted successfully, and several Master and PhD theses on NAVOLCHI technology have been initiated at partners' institutes.

3 Core of the Report

3.1 Project Objectives for the Period

WP1 (Project Management) Objectives

- Performing common project management tasks
- WEB-site continuous update,
- Admission of ETH as a new partner in the consortium as reaction on the retreat of ST from activities in work package 6
- Application for an extension of the project by six months to complete the development of fabrication processes.

WP2 (Interconnect Specifications) Objectives

- Implementation of VHDL model of serializer/deserializer.
- System modeling
- Design space exploration
- Device definitions and specifications of the sub-modules
- To define optical interconnection system environment and parameters within which the plasmonic devices have to function

WP3 (Plasmonic Transmitter) Objectives

The main objective of WP3 for the reporting period was to carry out the fabrication of the plasmonic transmitter. This component consists of two devices, which are a metal-cavity nanolaser and a plasmonic modulator, both coupled to photonic wire. Nevertheless, given the current progress on the individual devices and the technological challenges to integrate them, it has been identified that the project demonstrator will most likely have one of these devices. In a first scenario, an external laser will feed the plasmonic modulator, whereas a directly modulated metal-cavity nanolaser is considered as an alternative solution. The milestones corresponding to WP3 in the reported period are:

- Milestone 14: Initial testing and characterization of plasmonic modulators
- Milestone 15: Initial testing of bonded plasmonic lasers

WP4 (Plasmonic Receiver) Objectives

- Plasmonic Amplifier:
 - IR Quantum Dots (HgTe) with gain.
 - Plasmonic Amplifier concept by using polymers incorporating those IR QDs (optical injection).
 - Si based Plasmonic Amplifier platform incorporating those IR QDs (electrical injection).
- Photodetectors using QDs and metal nanostructures
 - PbS quantum dots absorbing light at telecom wavelengths and conductive films based on them.
 - Photodetectors based on these films reaching responsivities of around 0.1 A/W at telecom wavelengths: Schottky/heterostructure vs nanogap/microgap devices.
 - Design of nano-gap waveguide photoconductors.

WP5 (Optical and Electrical Interfaces) Objectives

- Fabrication and characterization of the metallic taper photonic-to-plasmonic mode converters
- More comprehensive theoretical study of the MMI based photonic-to-plasmonic mode converters
- Design of second generation beam shapers
- Implement new PHY adapter integrated with developments in WP2
- Initiation of FPGA implementation of signal generation module

WP6 (Integration, Characterising and Testing) Objectives

Characterization and testing of first active and passive plasmonic devices.

WP7 (Exploitation and Dissemination) Objectives

- Dissemination through paper submission to high quality and high impact scientific journals, magazines and white papers.
- Promotion of the project outputs through the participation in conferences and symposia.
- Organizing workshops/seminars on NAVOLCHI technology.
- Interaction with other EU-funded and national projects.
- Issuing of press releases and brochures.
- Generation of intellectual property (patents portfolio).
- Theses at the partners' institutes on NAVOLCHI technology.

- Provide input to industrial partners based on scenarios of the proposed solutions.
- Maintenance of the project web site which will be used for information and result dissemination purposes.

3.2 Work Progress and Achievements

3.2.1 Work Package 1: Project Management

Please refer to chapter 3.3 for a detailed description of the activities concerning the project management.

3.2.2 Work Package 2: Interconnect Specifications

This work package investigates the new plasmonic device technology for chip-to-chip interconnection.

General status

The progress of WP2 is generally on track. Deliverable D2.3 and D2.4 have been submitted. Milestones MS4, MS5 and MS6 were met, while milestone MS7 is in progress.

Task 2.1 has been completed, while T2.2 and T2.5 are in progress. Objectives have been met.

Task 2.2 Work Progress (Modelling of devices and system for communications applications)

The aim of this task is to give device specifications for the novel disruptive plasmonic Si-photonics devices and its application in the chip-to-chip interconnection environment.

A simulated model has been implemented that it is used for the design space exploration and the definition of the sub-system specifications. The simulation platform has been realized with the commercial VPI Photonics software. Eight different configurations have been studied in total: with direct or indirect modulation, with plasmonic or PIN detector, with or without amplifier. The Bit Error Rate has been calculated for each case, sweeping parameters such as the laser output power or the amplifier gain. The study is focused on the question of device characteristics, so that the system target specifications are achieved. The eight different configurations that have been studied is part of the design space exploration that has been performed in order to find the configuration that better meets the system requirements.

The simulated model includes the plasmonic transmitter, the plasmonic receiver and the channel. The plasmonic transmitter consists of a metallo-dielectric laser and a plasmonic modulator. The plasmonic receiver consists of a plasmonic pre-amplifier and a plasmonic photodetector. Gratings are used to couple light out of and into the chips.

The potential system configurations under investigation are shown in the following figures.

In Figure 2- 1 you can see the indirect modulation scenario. The metallic nanolaser feeds the plasmonic modulator. The modulator sends the modulated signal to the receiver chip, where it goes through the plasmonic amplifier before ending up in the photodetector. The laser, the modulator and

the receiver are on 3 different chips. The communication between the chips is established by gratings to send and receive the signal.

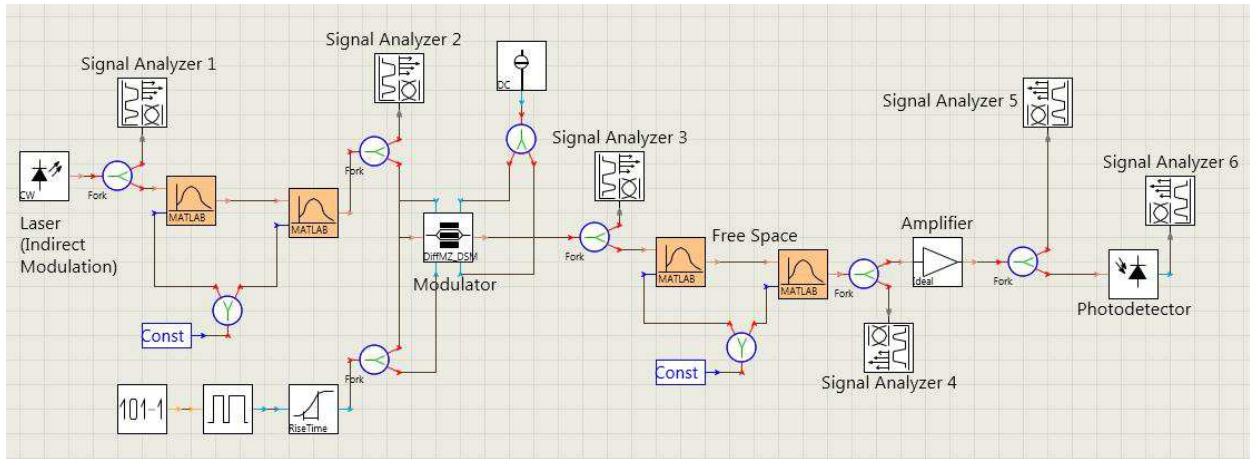


Figure 2- 1: Indirect modulation scenario with plasmonic amplifier.

The indirect modulation scenario is studied with two different photodetectors. A plasmonic one from UVEG and a standard PIN one from IMEC. In addition, each case will be studied with and without the amplifier. See the indirect modulation scenario without the amplifier in Figure 2- 2.

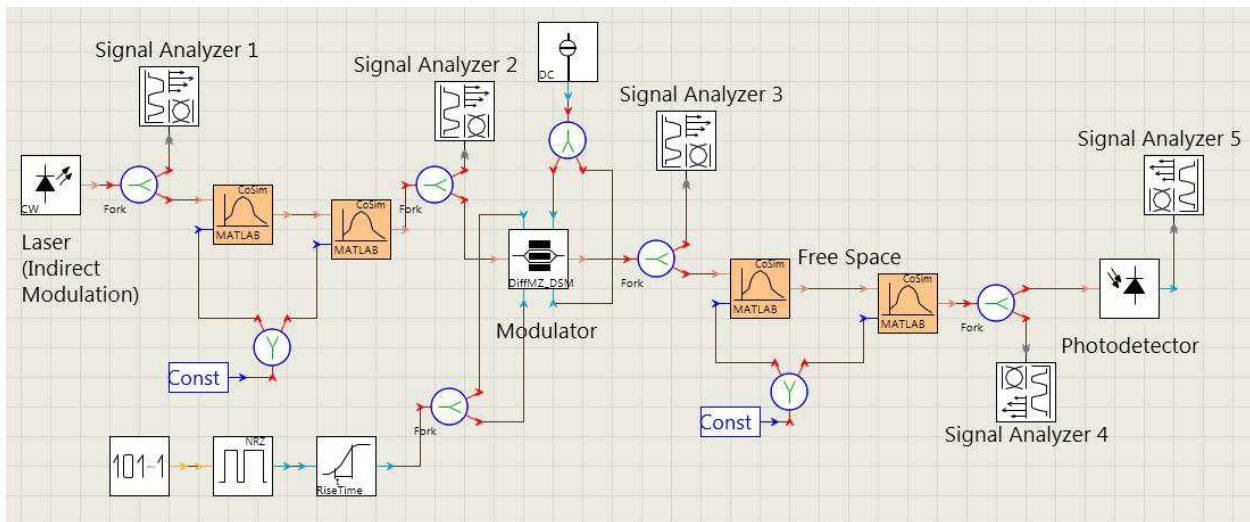


Figure 2- 2: Indirect modulation scenario without a plasmonic amplifier at the receiver.

Then, we studied the same system with direct modulation. The idea here was that the power of the metallo-dielectric laser is low ($\sim 50 \mu\text{W}$) and maybe that will not be enough to cooperate with the plasmonic modulator. The direct modulation scenario is shown in Figure 2- 3 and Figure 2- 4.

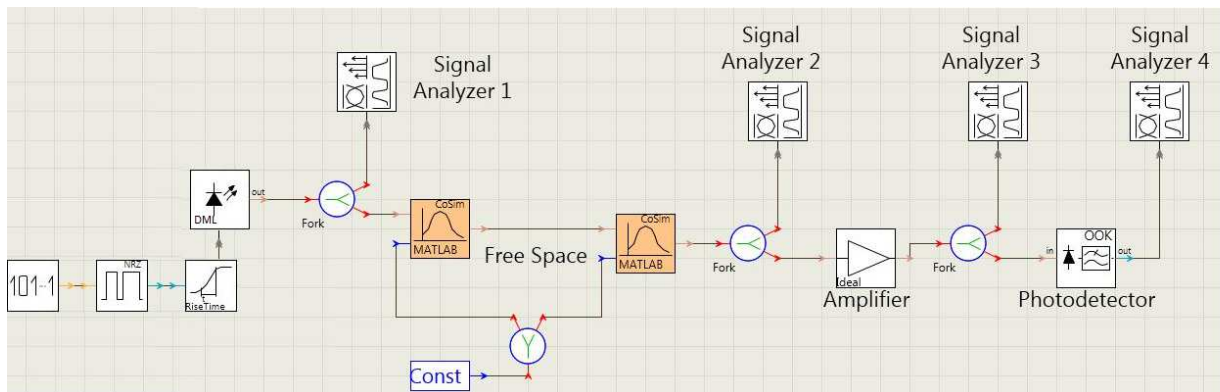


Figure 2- 3: Direct modulation scenario with plasmonic amplifier.

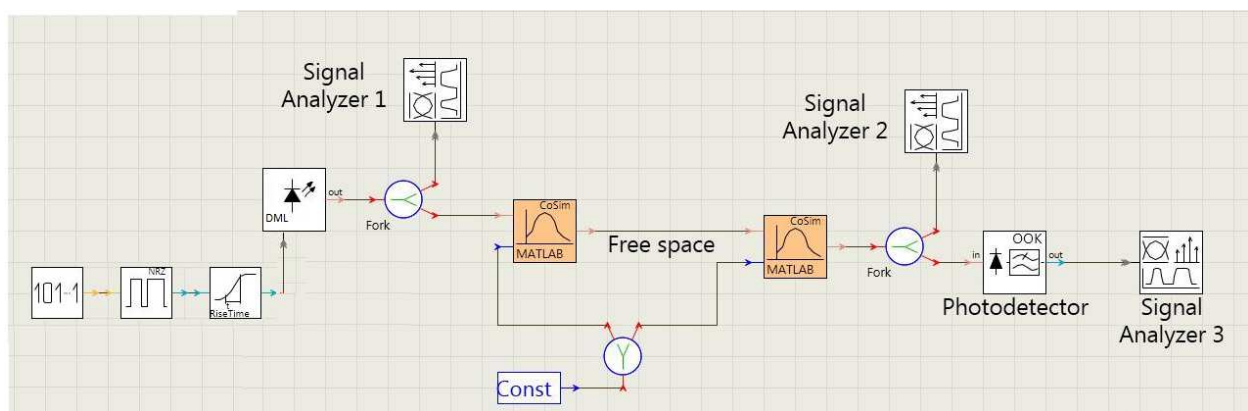


Figure 2- 4: Direct modulation scenario without plasmonic amplifier.

All scenarios have been simulated with the receiver comprising (a) PIN detector from IMEC, or (b) plasmonic detector developed at UVEG.

For all approaches, each device can be modeled either by changing the parameters that VPI provides or through Matlab (through the Cosimulation VPI package). Cosimulation enables us to implement new simulation modules, additional to those provided by VPIphotonics.

The detailed results of the simulated models are described in D2.3. The Bit Error Rate has been calculated for each case, sweeping parameters such as the laser output power or the amplifier gain. In the direct modulation case the signal phase distortions have not been taken into account due to lack of chirping information for the plasmonic devices. In addition, we noted that many of the device parameters used in the simulations are estimations at this point of development.

The results for the indirect modulation case show that the estimated metallo-dielectric laser (that is being developed within NAVOLCHI) output power is too low to receive an acceptable BER at the receiver end. Powers on the order of magnitude of mW are needed for error-free transmission this case, as opposed to the 50 μ W that the NAVOLCHI laser delivers. On the other hand, in the direct modulation scenario the 50 μ W of laser output power seem to be enough for error-free transmission.

In view of these results, it appears that 2 two different configurations will be studied in the final performance evaluation. In the first case the metallo-dielectric laser will be used with direct

modulation at the transmitter. In a second system, the plasmonic modulator can be paired with a commercial laser at the transmitter.

Task 2.3 work progress (Value analysis in terms of cost and green aspects [M25-M30])

This Task has just started and it is in progress. The first Milestone on this task is on M28.

Task 2.4 work progress Techno-economical evaluation and benchmarking [M24-36])

This Task has started and it is in progress.

Task 2.5 work progress: VHDL modelling of plasmonic interconnect and CMOS interface circuits [M10-M24]

(VHDL modeling on plasmonic interconnect and CMOS interface circuits [M10-M24])

The objective of this task is the implementation of behavioral models of the plasmonic devices (emitter, detector, modulator, transmission medium) and the CMOS mixed analog/digital circuits responsible for interfacing the digital modules with the plasmonic devices.

The task has been completed on time.

Last year a Verilog-A training has been followed by Alberto Scandurra (ST) on January the 30th/31st 2013 at the Agrate site of STMicroelectronics; Verilog-A is a Hardware Description Language (HDL) extending the classical Verilog language, specific for VLSI digital system, with capabilities for modeling analog electronic devices, as well as photonic, mechanical and thermal systems. This language was supposed to be used for modeling the plasmonic devices in terms of both functionality and physical effects conditioning their behavior (such as temperature variation impact on performance, etc.), and the analog electronic components allowing the digital electronic system to interact with the plasmonic devices, such as emitter/modulator driver, Trans-Impedance Amplifier (TIA), voltage level adjusters, and so on. However, while carrying out the task, it has been realized that using VHDL for modeling both plasmonic and analog parts at behavioral level was simpler and faster, in particular for what concerns co-simulation with the designed digital parts.

The modeling activity has been carried out between July and October 2013 exploiting a post graduate stage.

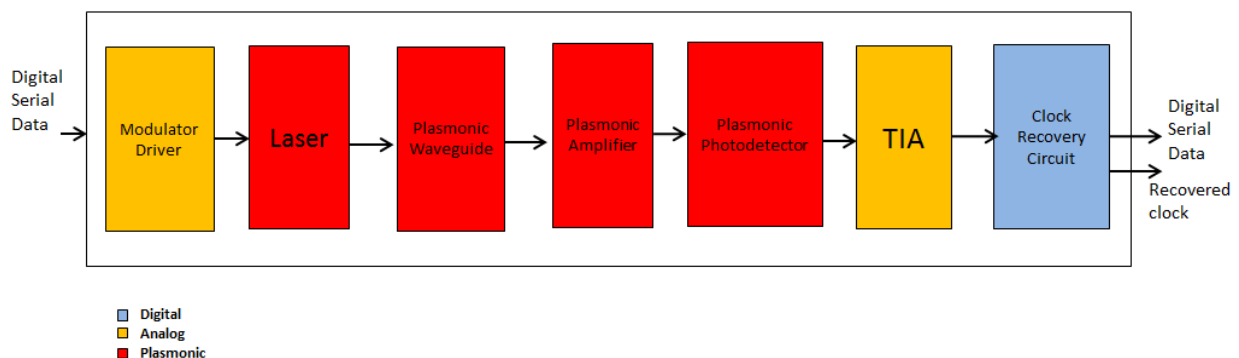


Figure 2- 5: Plasmonic Interconnect Block Diagram (Top-level).

As far as the interface circuits are concerned, they are the digital building-blocks that in the demonstrator will be mapped onto an FPGA in order to have a fast prototype available for plasmonic chip to chip interconnect characterization. These blocks are the serializer and the deserializer already developed last year, bi-synchronous FIFOs to store data and decouple the different clock domains (the slow one of the processing electronics and the fast one of the chip to chip communication) and a set of encoders and decoders allowing to minimize the power consumption (Optical Bus Inverter, Bus Inverter).

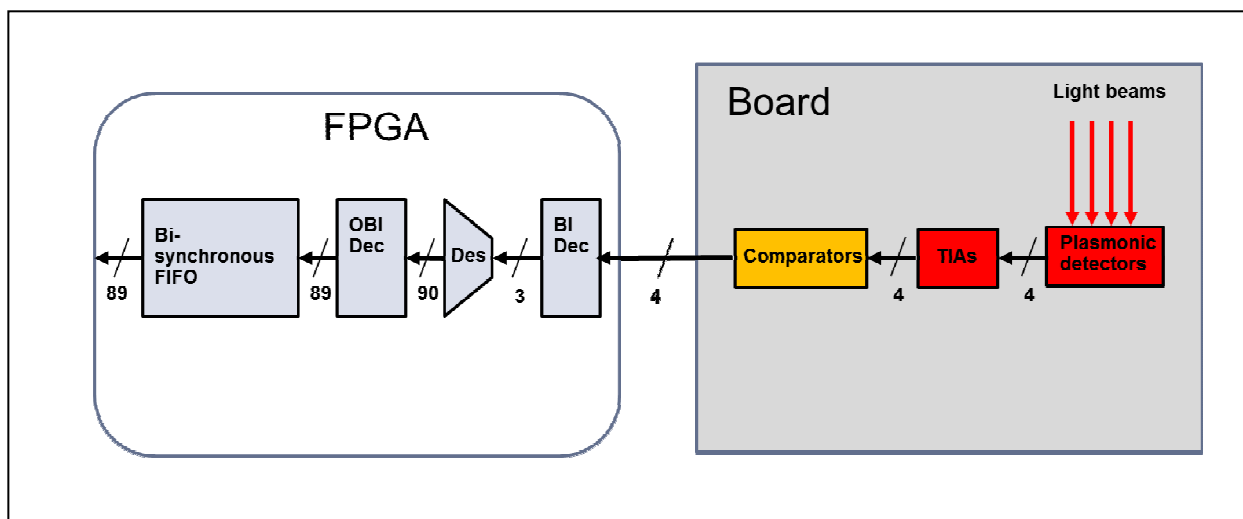
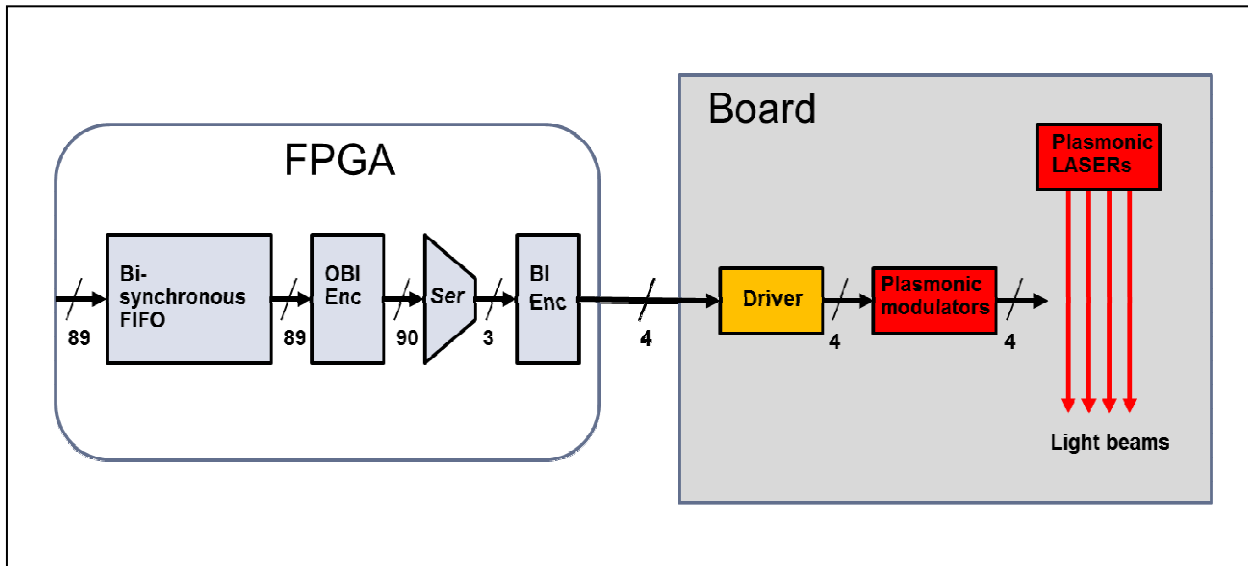


Figure 2- 6: NAVOLCHI demonstrator PHY adapter transmitter.

Milestones until month 24

MS4 Definition of the interconnection level specification employing developed plasmonic photonic devices (month 18) – Completed in time

MS5 Digital domain to plasmonic domain interface specification and VHDL modeling (month 21) – Completed with delay (month 23)

MS6 Plasmonic interconnect VHDL modeling (month 24) – Completed with delay (month 25)

Deliverables until month 27

D2.1 Definition of chip-to-chip interconnection system environment and specification (month 3) – Completed.

D2.2 Definition of plasmonic devices (month 12) – Completed.

D2.3 Investigation of chip-to-chip interconnection level specifications employing new plasmonic devices (M24)

D2.4 Interface and plasmonic interconnect models and reports (M24)

Upcoming deliverables

D2.5 Technoeconomical evaluation with respect to the cost efficiency and green aspects (M30)

D2.6 Report on new applications and their opportunities (M36)

Milestones until month 27

MS 1 Definition of chip-to-chip interconnection system environment and specification (month 3) – Completed.

MS 2 Definition of plasmonic devices and material properties for chip-to-chip interconnection (month 6) – Completed.

MS 3 Development of a system and device simulation platform (month 18) – Completed.

MS 4 Definition Derivation of the interconnection level specification (month 18) – Delayed (estimated date: July 2013)

MS 5 Digital domain to plasmonic domain interface specification and VHDL modeling (month 21)

MS 6 Plasmonic interconnect VHDL modeling (month 24)

Upcoming Milestones

MS 7 Investigation of the cost and power consumption efficiency of the developed plasmonic devices and systems (month 28) – No delay expected.

3.2.3 Work Package 3: Plasmonic Transmitter

Task 3.3. Fabrication of plasmonic nanolaser

1. Introduction

We proposed in D3.1 a metal-cavity nanopillar structure coupled by an evanescent field to an InP-membrane waveguide as shown in Figure 3- 1 [1]. Both the laser and waveguide are fabricated in a III-V layer stack bonded to a silicon substrate with Benzocyclobutene (BCB) [2]. The pillar has an undercut above and below the active region (InGaAs) to increase the cavity quality factor. It is covered by a dielectric layer and then encapsulated with silver to form the metal-cavity that provides a strong feedback to the TE mode supported by the cavity. The metal cladding makes electric contact on the top of the pillar, whereas a lateral p-contact is deployed over a large area to minimize its contact resistance. We also include a grating coupler to couple the light out of the chip.

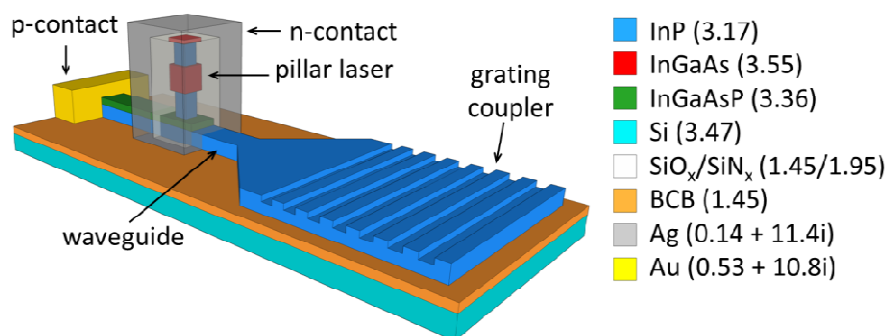


Figure 3- 1: Schematic of a metal-cavity nanolaser coupled to an InP-membrane waveguide connected to a grating coupler. The refractive index of each material at 1.55 μm is shown in parenthesis.

The present report gives an overview of the fabrication technology we have developed to fabricate this nanolaser. Firstly, the generic technology developed for III-V samples (not bonded to silicon) is presented. Next, the fabrication results of the first run carried out in III-V samples bonded to silicon are summarized, as well as the issues and challenges we encountered.

2. Technology development for III-V wafers

2.1. Electron-beam lithography and etching processes

The definition of the nanostructure is carried out by electron-beam lithography (EBL) due to the high resolution required. This is done in three EBL steps. During the first lithography, the nanopillar is defined. Later, an overlay exposure is needed to define the waveguide and, finally, the grating coupler is defined with another overlay exposure. Three different lithographic masking schemes are used during these EBL steps, which are depicted in Figure 3- 2 (left) and discussed in the following.

The first EBL exposure is done using HSQ resist, which is a negative resist well known for its usage in high resolution lithography [3]. Since it can be thinner than 100 nm, the influence of the electron scattering inside the resist is limited. However, its thickness is not enough to etch a hardmask able to withstand the etching of the pillar (about one micrometer high), and therefore it has to be used in combination with another resist in a bilayer resist scheme in order to be able to etch high aspect ratio structures [4]. The pattern in HSQ is transferred to an underlying HPR504 resist by means of a reactive-ion-etching (RIE) process using oxygen, which in turn is used to transfer the pattern into a SiO_x layer with a CHF₃-based RIE step. Finally, the SiO_x is used as a hardmask to etch the semiconductor pillar with inductively coupled plasma RIE (ICP-RIE) using a methane-hydrogen chemistry (CH₄:H₂).

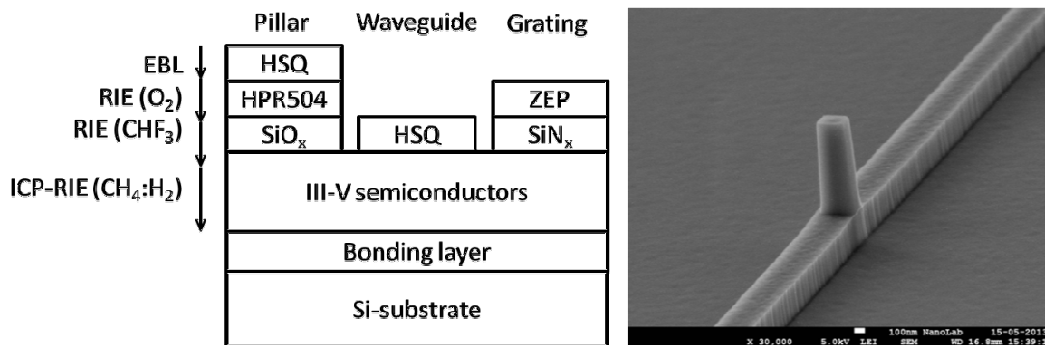


Figure 3- 2: Left: Processing schemes to fabricate the nanostructures. The top layer of each lithographic scheme is always defined by EBL and development. Right: Pillar after waveguide etching and removal of hardmasks.

In a second EBL exposure, the waveguide is defined at the bottom of the pillar structure. During this step, a mask protection for the pillar is mandatory, otherwise the pillar will be eroded during the waveguides etching. For this purpose, the hardmask to etch the pillar is not removed after the first lithography.

An overlay EBL normally demands a prior planarization of the surface to keep the resist thickness uniform as well as the hardmask layer. We avoid such planarization by using the HSQ resist directly as the hardmask. This technique requires enhancing the resistance of HSQ to the semiconductor etching chemistry used in the RIE, which can be done either by hard curing HSQ [5] or by treating it with an oxygen plasma [6]. In this way, after the pillars have been etched, HSQ is spun, e-beam exposed, developed, and treated with an O₂-plasma. Later, this HSQ is used as the hardmask to etch the waveguide using methane hydrogen in a RIE process. The result of these two lithography steps is shown in Figure 3- 2 (right). The figure shows that despite the large surface topology introduced by the pillar, the definition of the hardmask at the waveguide level is very good.

A final e-beam lithography is required to fabricate the grating coupler. In this case, ZEP resist in combination with a SiN_x mask is used. This is preferred because it is a positive resist, which means that any non-exposed region (i.e. the pillar and waveguide) will be protected by the SiN_x hardmask during the grating etching. The undercut to enhance the quality factor of the cavity, as described in our laser design [1], can be fabricated right after the pillar etching by a selective wet etching of InP as it is shown in Figure 3- 3.

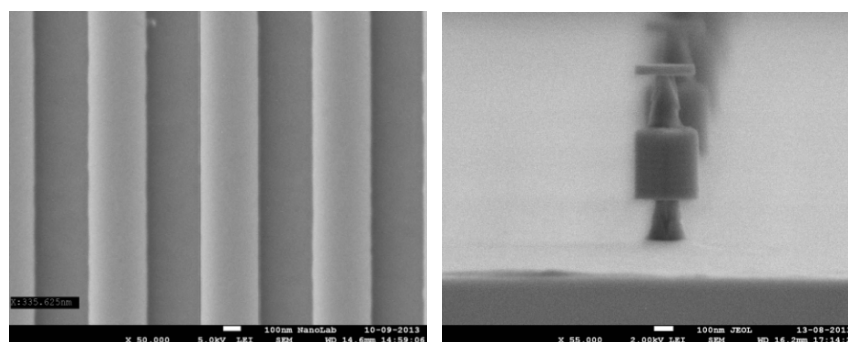


Figure 3- 3: Left: Top view of a typical grating coupler. Right: Pillar with undercut fabricated using the solution H₂O:H₃PO₄:HCl.

2.2. Deposition of dielectrics and metals

The metal cladding of the cavity would create a short circuit unless a dielectric layer is deposited before the silver, which also helps to reduce the metal loss as predicted by the design simulations [1]. For this purpose, either SiN_x or SiO_x can be deposited by plasma-enhanced chemical vapor deposition (PECVD), however it has been found that a SiO_x cladding will result in a higher quality factor due to its lower refractive index. Before the actual deposition of the chosen dielectric, a thin passivation layer of SiN_x of a few nanometers can be deposited at low temperatures to reduce the surface recombination [7]. Since the resonant wavelength is mainly given by the cavity size (thickness of the dielectric cladding plus the semiconductor pillar width), it is important to take into account that the PECVD deposition rate on sidewalls is about two thirds of the deposition rate on a flat surface.

After the pillar has been covered with a dielectric layer, silver can be thermally evaporated to form the metal-cavity. However, since silver does not stick on $\text{SiO}_x/\text{SiN}_x$, an adhesion layer must be deposited in advance by lift-off, for example Ti/Au, chromium [8] or germanium. In order to cover the sidewalls of the pillar, the silver evaporation should be done at various angles. Since the evaporation leads to the formation of silver grains, rapid thermal annealing (RTA) is applied after the evaporation to increase the metal grain size resulting in a more uniform metal with reduced scattering loss. Figure 3- 4 shows a pillar covered with silver before and after RTA at 400 °C.

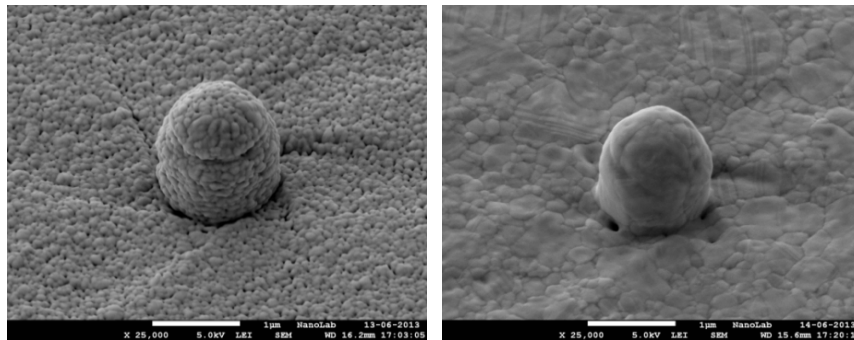


Figure 3- 4: Left: Pillar after silver evaporation. Silver grains of about 30 nm are formed. Right: Silver-covered pillar after RTA. These tests were done using non-bonded InP wafers.

3. Results of first laser run in III-V samples bonded to silicon

After developing the main technology processes for the fabrication of the waveguide-coupled nanolasers, we carried out a first fabrication run of lasers on bonded samples. Deliverable 3.3 reports the complete process flow used for this first run. In this section, we describe the main issues we have encountered during such a run, and the way in which we are going to solve them.

The first issue we had has to do with the verticality of the pillars, which will lead to a decrease in the quality factor of the optical cavity. As can be seen in Figure 3- 5, we obtained non-vertical pillars during the ICP-RIE etching with a methane-hydrogen chemistry at 60 °C. We believe that it is due to heating of the sample during the etching because of the low thermal conductivity of the BCB bonding layer. We will optimize the etching recipe to get a higher verticality in bonded samples, by reducing either the RF power to generate the plasma or by reducing the substrate temperature.

Another issue is that the top of the pillars are not completely protected during the grating coupler etching, which results in etching of the pillar top as seen in Figure 3- 5 (right). In a next run we plan

to protect the pillars during the gratings etching with photoresist, which involves an additional non-critical optical lithography step.

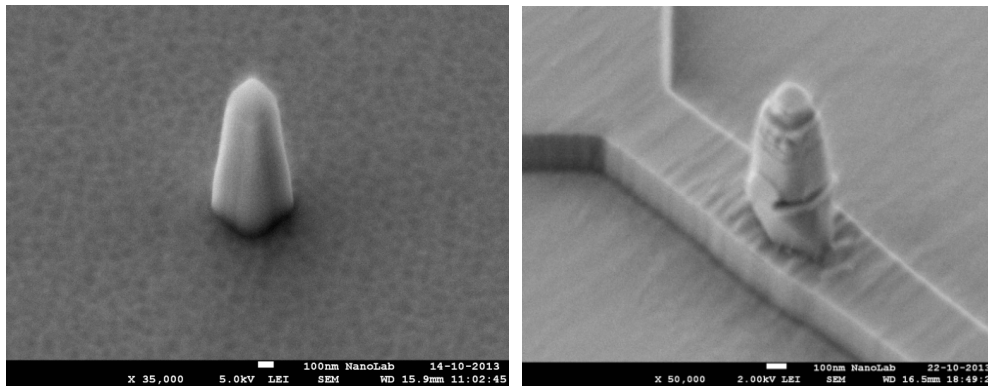


Figure 3- 5: Left: non-vertical pillar etched in a III-V sample bonded to silicon. Right: Pillar on top of a waveguide, whose top has been etched.

After the etching of pillar, waveguide and grating coupler, the pillar has to be covered by SiO_x , as described previously. The roughness of the present process will degrade the quality factor of the cavity due to optical scattering. Figure 3- 6 (left) shows a pillar covered with SiO_x , which shows large roughness. We are currently optimizing the recipe to improve the quality of the dielectric.

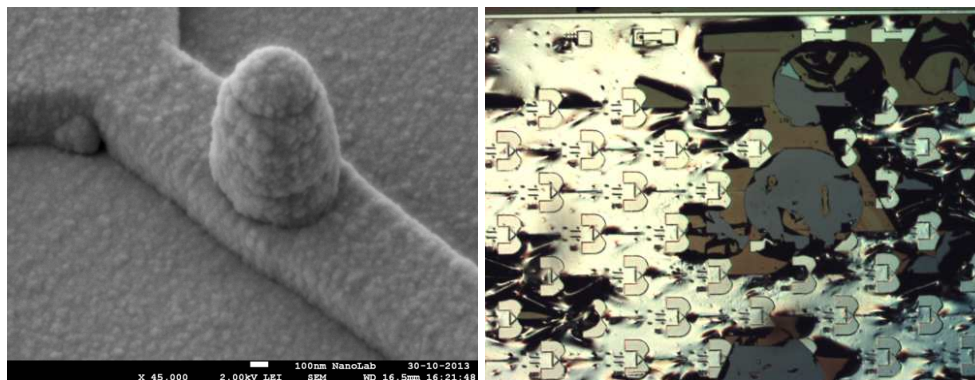


Figure 3- 6: Left: Pillar on top of waveguide covered with a rough SiO_x . Right: Round defects in sample presumably produced by BCB outgassing during thermal annealing at high temperatures.

Finally, another issue happens during the annealing of the silver needed to increase the grain size and improving its quality. After doing RTA above 400 °C, circular defects were observed, which lift off the previously deposited silver. The circular shape, suggests that it is due to outgassing of the BCB bonding layer. We plan to reduce the annealing temperature, such that it will still improve the silver quality, but without producing significant BCB outgassing. Further, we will cure the BCB at higher temperatures during the bonding process, so that it is not affected anymore during the annealing process. This is one of the most critical issues to solve in the future, since we require both a high quality silver (which we achieve by annealing at high temperatures) and a III-V sample bonded to silicon by means of BCB (which works best at lower temperatures).

4. Conclusions

The main technology and fabrication techniques developed to fabricate the nanolaser have been described in this section. Additionally, the results of the first run of lasers on III-V samples bonded to silicon were presented. The fabrication issues encountered in the processing of bonded samples were discussed as well as the ideas how to solve them.

5. References

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- [8] J. Hyoung Lee, “Electrically pumped sub-wavelength metallo-dielectric pedestal pillar lasers”, *Optics Express* 19(22), pp. 21524-21531, 2011

Task 3.4. Fabrication of Si-plasmonic modulators

1. Introduction

Two modulator structures have been successfully fabricated within NAVOLCHI - namely the surface plasmon polariton absorption modulator [1,2], where the intensity of SPP is directly modulated by plasma effect in metal oxide, and surface plasmon polariton phase modulator [3,4], where the phase of SPP is modulated making use of the Pockels effect, see Figure 3- 7.

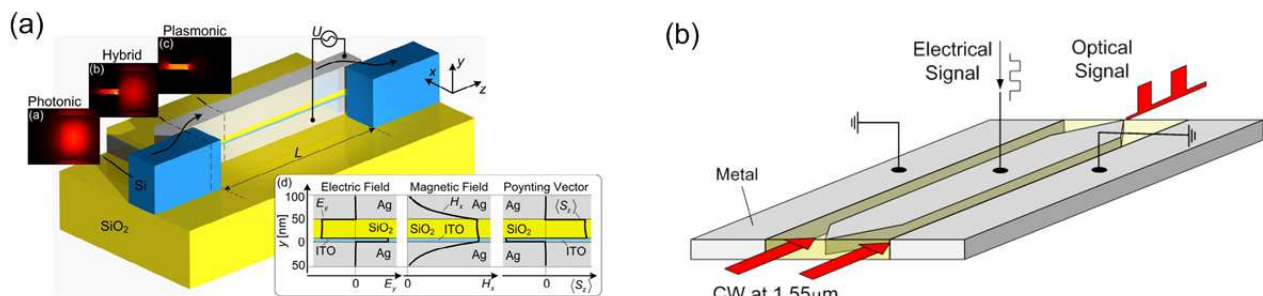


Figure 3- 7: Plasmonic modulator approaches engaged by NAVOLCHI. (a) Surface plasmon polariton absorption modulator [1,2] and (b) plasmonic phase modulator[3,4].

2. Plasmonic phase modulator

We have successfully fabricated two generations of plasmonic phase modulators, which show ultrawide RF and optical bandwidths. The modulators are tested for up to 40Gbit/s data modulations and the results are accepted for publication in Nature Photonics [4].

The fabrication of single plasmonic phase modulator has been successfully carried out by IMEC and KIT, by dividing the entire fabrication process flow into three steps

- Mask design for the fabrication of silicon/plasmonic platform
- Fabrication of passive silicon on insulator (SOI) chips at IMEC
- Fabrication of active plasmonic parts at KIT

KIT has designed a mask for the fabrication of the passive silicon platform to be further post-processed in order to define the metallic parts of the modulator. The entire mask layout occupies $3 \times 3 \text{ mm}^2$ area. Two standard diffraction grating couplers are used to couple light in and out the silicon nanowire waveguides. The important parts of the mask are the silicon taper pairs with various separations from $2 \mu\text{m}$ to $45 \mu\text{m}$, see **Milestone 25** “Decision on optimized plasmonic waveguide couplers”. The silicon tapers have tapering angle of 15° and tip size of 120 nm .

Silicon on insulator (SOI) wafer with a buried oxide layer thickness of $2 \mu\text{m}$ has been processed by IMEC. Si nanowire waveguides with a height of 220 nm and a width of 450 nm are fabricated with a 193 nm DUV lithography followed by Si dry etching, see Figure 3- 8. Silicon tapers with a

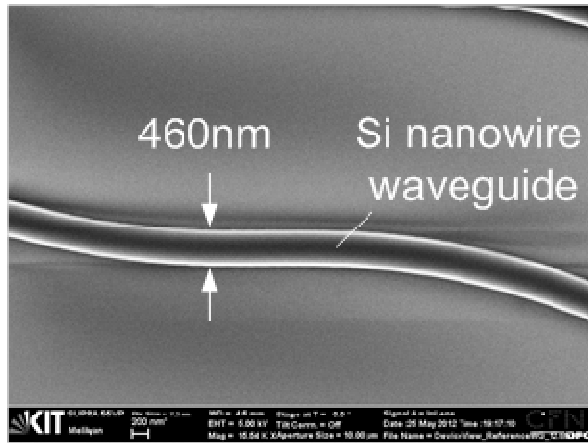


Figure 3- 8: Scanning electron microscope image of the fabricated silicon nanowire waveguide

taper angle of 15° and a tip size of 147 nm are structured in the final etching process, see Figure 3- 9. The metallic slot waveguides are fabricated by a standard lift-off process with PMMA e-beam resist. A 150 nm thick gold layer is evaporated onto the samples by an electron beam evaporation system, see Figure 3- 10. After completing the lift-off process the samples are coated with the commercially available polymer M3 having a maximum electro-optic coefficient of $r_{33} = 70 \text{ pm} / \text{V}$ [5]. The electro-optic property of the polymer is then activated by a poling procedure, where a static electric field aligns the randomly oriented dipole moments of the chromophores at an elevated temperature [6]. After rapid cooling to room temperature, the ordering of the dipole moments pertains even after removal of the electric field.

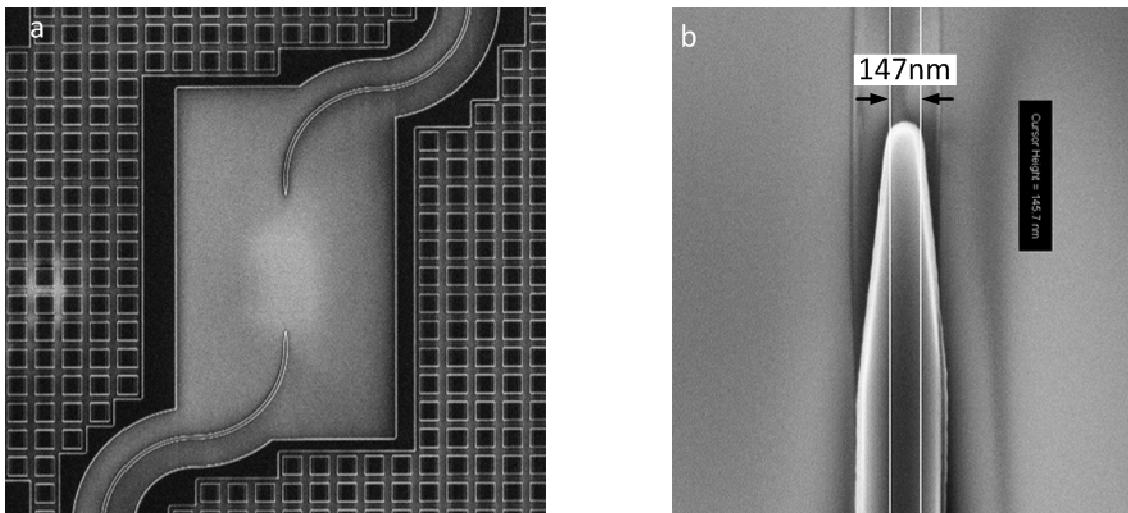


Figure 3- 9: Fabricated passive silicon platform. (a) Fabricated pair silicon tapers which will be used for light coupling in and out from the plasmonic modulator. (b) Fabricated silicon taper. Designed tip size of 120 nm resulted in 150 nm tip size.

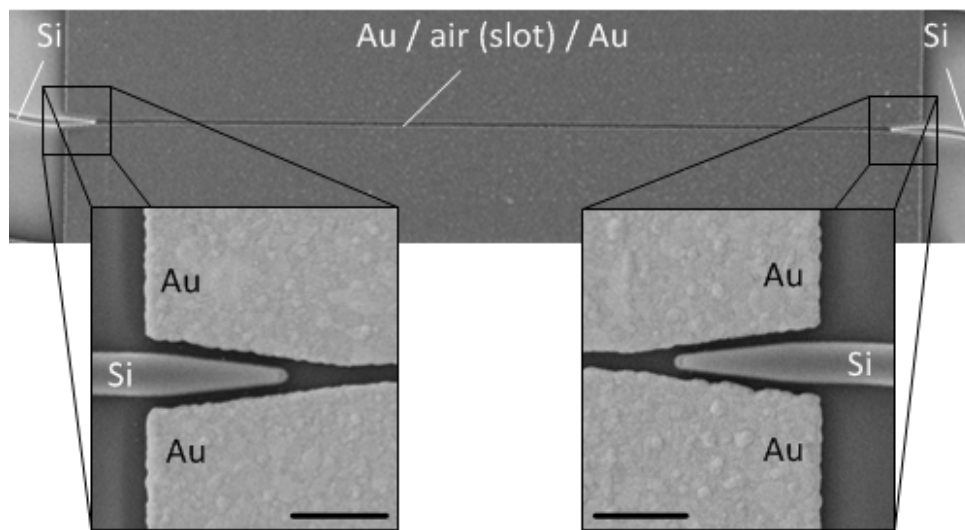


Figure 3- 10: Scanning electron microscope image of the fabricated plasmonic phase modulator. The photograph is taken before coating with an electrooptic polymer. Black bars are one micrometre.

3. Plasmonic absorption modulator

We have successfully fabricated the first generation of plasmonic absorption modulators which already show good switching behaviour with an extinction ratio of 6dB for 3V applied voltage. The results have been submitted to CLEO2014[2].

The surface plasmon polariton absorption modulator (SPPAM) is designed on a standard silicon-on-insulator (SOI) platform. The core of the device is the active material indium-tin-oxide (ITO), since the carrier density and thus, the absorption of ITO may be switched by applying an electrical field. The modulator comprises a metal-oxide-ITO-silicon layer stack guiding a hybrid surface plasmon polariton, see Figure 3- 11.

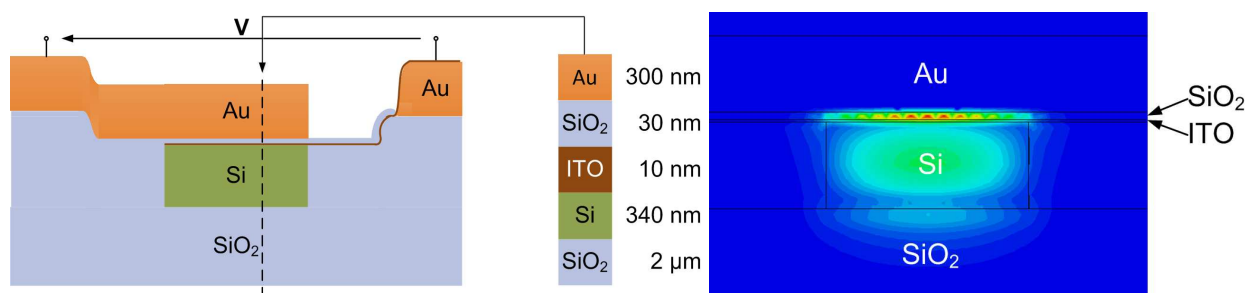


Figure 3- 11: Cross section of the plasmonic absorption modulator comprising a metal-oxide-ITO-silicon layer stack and the plasmonic hybrid mode in the modulator section.

The mask layout for the SPPAM comprises modulator of various device lengths (3 μm, 5 μm, 10 μm and 20 μm). Besides single devices, there are modulator arrays of two and four channels with pitches of 35 μm, 50 μm and 250 μm. Furthermore, the layout includes purely passive devices to determine the corresponding losses.

Figure 3- 12 shows a modulator array with four channels. The red areas are the passive silicon components. All passive devices are designed for a height of 340 nm and TM polarized light. They can be fabricated in a single etch step. The light is coupled to the chip via grating couplers (GC, period 840 nm, fillfactor 0.6). It is then guided by 800 nm wide waveguides and split into several

arms with multimode interference (MMI) devices of $8.39 \mu\text{m}$ length. The modulators are electrically contacted by means of gold pads ($60 \mu\text{m}$ by $100 \mu\text{m}$), indicated by the blue areas.

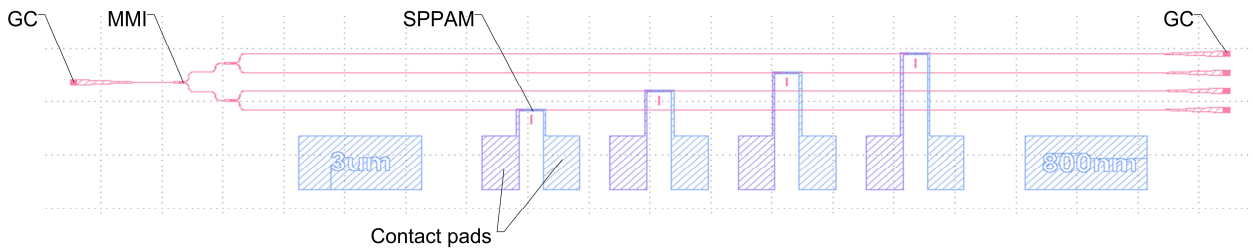


Figure 3- 12: Mask layout for the fabrication of an SPPAM array on an SOI platform.

The fabrication process in detail is described in **Deliverable D3.4** “*Report on fabrication of modulators*”. Figure 3- 13 shows an optical microscope image of fabricated modulator arrays with four channels and various device lengths. A close-up of a $5 \mu\text{m}$ long single device can be seen in Figure 3- 14. The SEM image given in Figure 3- 15, shows a cross section of the SPPAM. The rectangle in the middle is the silicon waveguide with the thin—and therefore barely visible—ITO and SiO_2 layers on top. The bottom electrode is shifted with respect to the top electrode. The trenches are caused by the fact that the cladding deposition on top of the silicon waveguide leads to a bump in the oxide layer. This bump is transferred when opening the oxide in the following step.

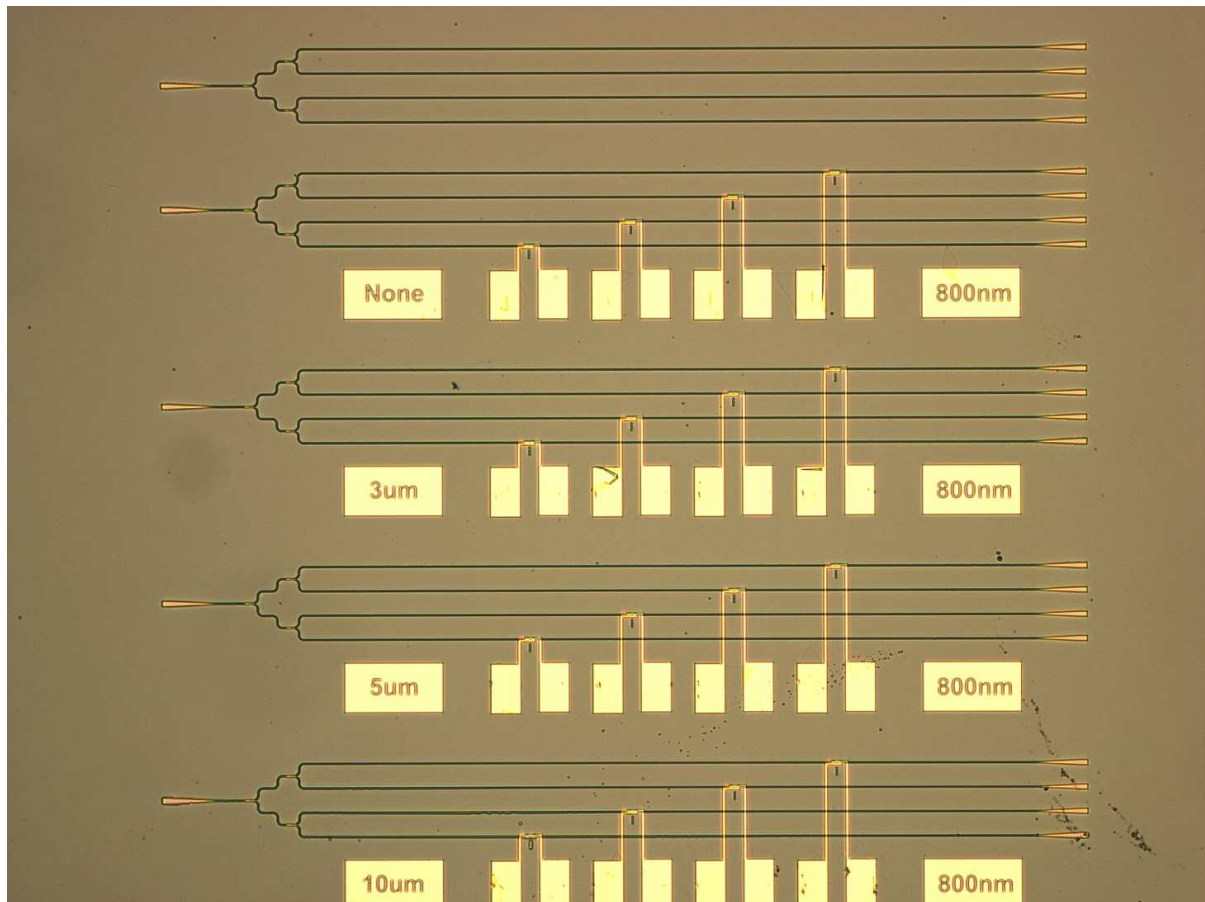


Figure 3- 13: Optical microscope image of fabricated SPPAM arrays with various device lengths.

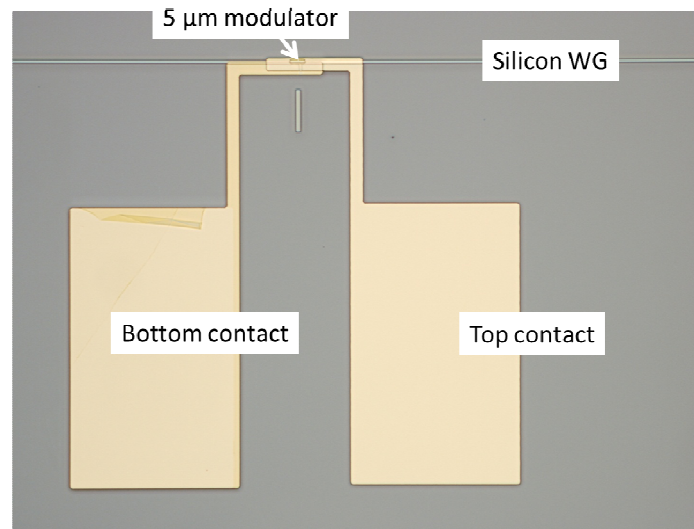


Figure 3- 14: Optical microscope image of a 5 μm long SPPAM

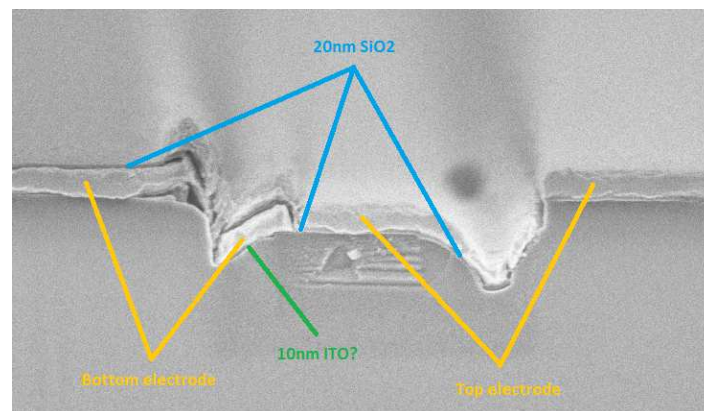


Figure 3- 15: Cross section of a fabricated SPPAM (SEM image)

4. References

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Deliverables in second intermediate reporting period (month 19 – month 27)

Deliverable	Name of deliverable	Responsible partner	Delivery date
D3.3	Fabrication of plasmonic laser device	TU/e	10/2013
D3.4	Report on fabrication of modulators	KIT	10/2013

Comments on upcoming deliverables related to WP3:

- TU/e is responsible for D6.1 “Report on characterization results of all plasmonic devices” which is part of WP6 and was planned to be delivered in month 27. Nevertheless, since there is a clear delay in the experimental demonstration of the nanolaser as well as a low loss plasmonic amplifier, the delivery of this report is planned to be shifted six months to match with the project extension that will be requested.

Milestones in second intermediate reporting period (month 19 – month 27)

Milestone	Name of deliverable	Responsible partner	Delivery date
MS14	Initial testing and characterization of plasmonic modulators	KIT	10/2013
MS15	Initial testing of bonded plasmonic lasers	TU/e	10/2013

3.2.4 Work Package 4: Plasmonic Receiver

Task 4.1 Design and modeling of plasmonic pre-amplifier

Task 4.1 Design and modeling of plasmonic pre-amplifier

a) Polymer based version

Task completed. The work at the moment is focused on fabrication and test of plasmonic structures previously determined as the best ones:

- Bilayer waveguide structures can improve the pumping conditions and the integration of the device, because it allows the coupling of the pump beam from the input edge of the sample.
- 2D waveguides are expected to improve the mode confinement.

b) Hybrid silicon plasmonic amplifier

Task completed.

Task 4.2 Modelling of plasmonic QD polymer based photodetectors

During the last months modelling of a plasmonic-waveguide nanogap photodetector was carried out, as incorporated in D4.3. This kind of photoconductor device will have advantages over a practically punctual nanogap photodetector using a bow-tie type design: it can detect light under normal incidence and in-plane coupling configuration, as illustrated in Figure 4- 1.

The electric field concentrates in the gap region and several intensity maxima are observed, as shown in Figure 4- 1, because a surface plasmon polariton standing wave develops when increasing the length of the nanogap plasmonic waveguide (as compared to the test wavelength, 1550 nm in the simulation) in contrast to the localized nature of the surface plasmon in a bowtie nanoantenna. The intensity enhancement inside the nanogap region is increasing in importance below 100 nm distance, being around a factor 30 in the case of a 50 nm nanogap value (reachable by fabrication, as recently demonstrated in the proofs developed by TUE), as shown in Figure 4- 1. It is worth to mention that the intensity maxima inside the nanogap does not exhibit attenuation (some kind of diffraction effect is observed in the simulation of in-plane incident light), what means that we can define the length of the nanogap waveguide as the most appropriate for integration purposes in silicon photonic circuits. The simulation was performed by considering the nanogap plasmonic waveguide on top of a SiO₂ substrate and air on top. We would like to consider a more realistic approach when working as a photodetector that consist in the cladding of the plasmonic structure by a semiconductor medium (PbS material), but at the moment was not possible by memory and processor limitations of our computer (that will be expanded/enhanced in brief).

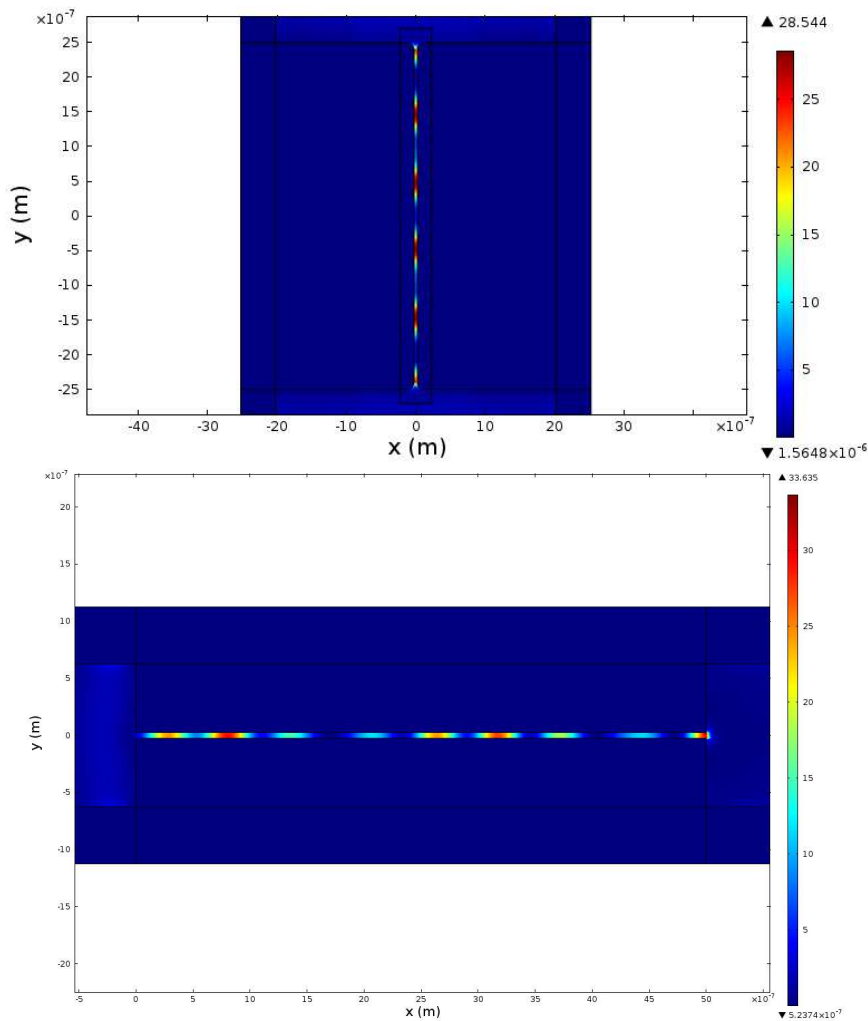


Figure 4- 1: Distribution of electric field intensity at 1550 nm in a nanogap plasmonic waveguide 5 μm long and gap distance equal to 50 nm for vertical (top panel) and in-plane (bottom panel) incident light.

The fabrication layouts and process definition of the nanogap plasmonic waveguide photoconductor with nanogap as short as possible (30-50 nm) and electrode length 2 - 5 μm was prepared (see Figure 4- 2: Fabrication layouts for the fabrication of nanogap plasmonic waveguide photoconductors. In dotted area is indicated the fabrication by using ebeam lithography.) and discussed with TUE group for its fabrication. A first generation of such plasmonic structures has been fabricated recently by TUE and subsequent processing for defining pad electrodes and QD deposition is under way at UVEG.

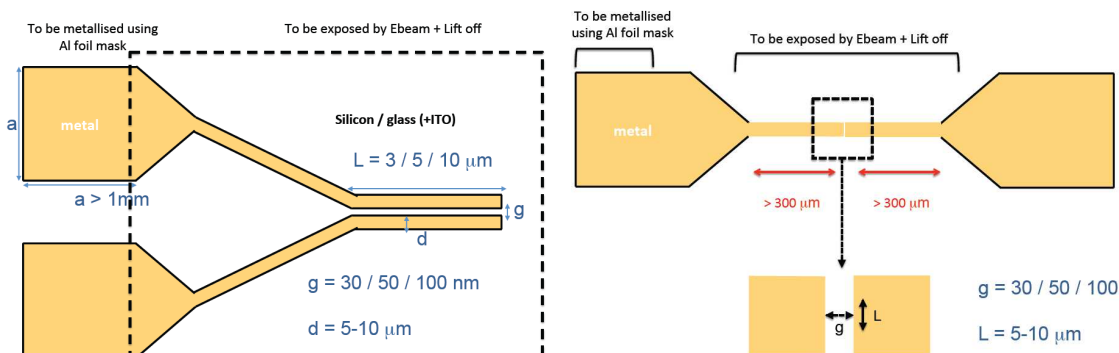


Figure 4- 2: Fabrication layouts for the fabrication of nanogap plasmonic waveguide photoconductors. In dotted area is indicated the fabrication by using ebeam lithography.

Task 4.3 Colloidal quantum dots with optimized gain and electrical injection scheme

a) Synthesis of HgTe based QDs

HgTe QDs were synthesized using a procedure adapted from literature:

- S. Keuleyan et al., “*Synthesis of Colloidal HgTe Quantum Dots for Narrow Mid-IR Emission and Detection*”, J. Am. Chem. Soc. **133**, 16422–16424 (2011).
- S. Kim_ et al. “*Bandgap engineered monodisperse and stable mercury telluride quantum dots and their application for near-infrared photodetection*”, J. Mater. Chem. **21**, 15232–15236 (2011).

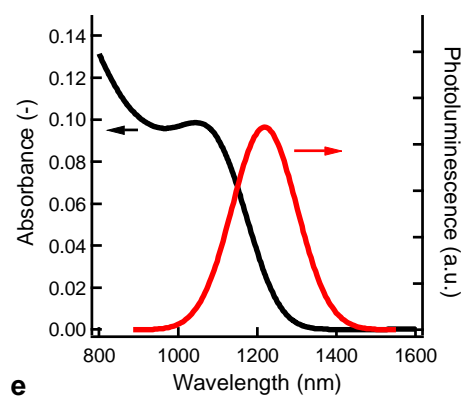


Figure 4- 3: Absorption and photoluminescence spectra of a colloidal solution of HgTe QDs.

The absorption and emission spectra of a colloidal solution of HgTe QDs feature the typical characteristics of the first exciton transition, albeit with a large apparent Stokes shift (120 meV for the data shown) between emission and absorption, as shown in Figure 4- 3. By changing the reaction conditions, the absorption and emission spectrum can be tuned throughout the entire near-infrared spectrum (from 1100 nm to 1600 nm). Time-resolved photoluminescence shows a non-exponential decay, which can be fitted using a double exponential with a short 30-40 ns and a longer 75 ns decay time. This is a very important difference with the earlier studied PbS based QDs which had 2 to 3 orders of magnitude larger lifetimes.

b) Light absorption in hybrid silicon-on-insulator/quantum dot waveguides

While waiting for the optimized HgTe QDs that can be embedded in the hybrid amplifier, we measured the transmission through SiN waveguides with an embedded layer of QDs deposited using the Langmuir-Blodgett method. The picture in Figure 4- 4 shows SEM top and cross-sectional views of the fabricated waveguides. The QD-layer is embedded between two layers of SiN (100nm thickness each), whereby the second layer (on top of the QDs) is deposited using a low temperature process. Afterwards the waveguides are defined using a standard etching process (optical lithography + RIE). As can be seen in the measured curves (Figure 4- 4), adding the QD layer increases the waveguide loss by approximately 1dB/cm. This should be no issue for the amplifier.

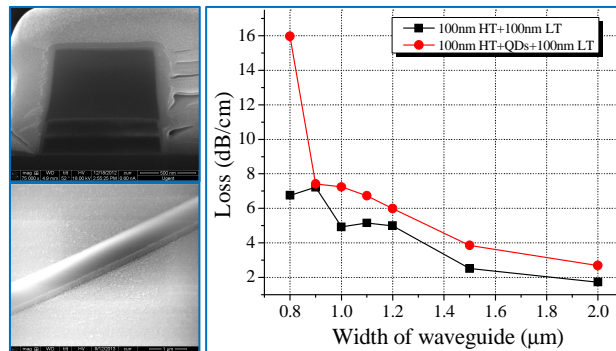


Figure 4- 4: Left: SEM cross-section and top views of fabricated waveguide structure (photoresists still on top). Right: measured propagation loss as function of the waveguide width for waveguide structures with (red) and without (black) embedded QD layer.

c) Gain characterization in solution

Two samples, with emission peak at 1220 nm and at 1300 nm resp. were investigated in detail using ultrafast pump-probe absorption spectroscopy. The results are described in detail in the paper attached as an appendix of MS22, which is currently being prepared for submission.

Figure 4- 5a shows the absorption spectra measured after photo-excitation, for different pump powers. The numbers indicated next to the curves indicate the average exciton population level $\langle N \rangle$ of the individual quantum dots. The region of the curves exhibiting negative values of the absorption (shaded areas in Figure 4- 5a) correspond to gain. This figure shows there is gain for excitations as low as $\langle N \rangle = 0.03$ exciton/dot, which is at least 1 order of magnitude lower than what was ever shown for any QD.

Figure 5b shows the intrinsic material gain expected for HgTe QDs under optical pumping (blue and red for QDs emitting at 1220 and 1300 nm, respectively). As an extrapolation, in an optical film, we have of course to take into account the fill factor of the film. Assuming a close-packed film a peak gain of 100 cm^{-1} (or 400 dB/cm) is extracted from the measurements in Figure 4- 5a.

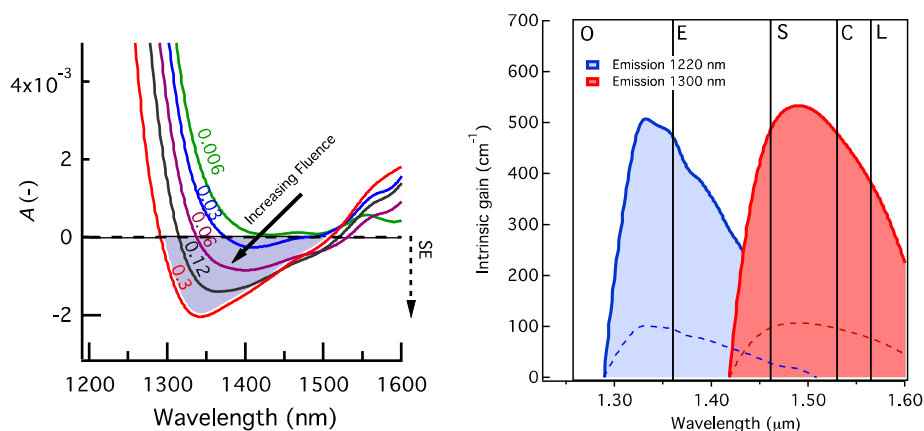


Figure 4- 5: a) Absorption spectra A , taken 2.5 ns after photo-excitation; stimulated emission (SE) corresponds to $A < 0$. The maximum gain bandwidth extends from 1310 to 1500 nm at a sub-exciton laser fluence ($\langle N \rangle = 0.3$). b) HgTe intrinsic material gain for two different samples emitting at 1220 nm (blue) and 1300 nm (red). The color-matching dashed lines indicate the volume-fraction corrected material gain. Note that the material gain provided by only 2 different sizes of HgTe covers the entire OESCL band with typical values over 100 cm^{-1} .

d) Gain characterization in dielectric films

The new and promising QD-material (HgTe) developed by UGENT, whose synthesis and gain characterization in solution was summarized above, was also studied embedded into PMMA to form optical waveguides on a SiO_2/Si substrate, as depicted in Figure 4- 6. In Structure I (Figure 4- 6a) the QDs are dispersed homogeneously in the PMMA matrix and in Structure II (Figure 4- 6b) a dense close-packed HgTe layer is deposited in between two PMMA layers. These waveguides have been characterized by end-fire coupling and by the variable stripe length method in order to examine their waveguide photoluminescence, gain and losses (as similarly reported for other QD-materials in deliverable 4.1) under continuous wave (CW) and pulsed laser pumping conditions.

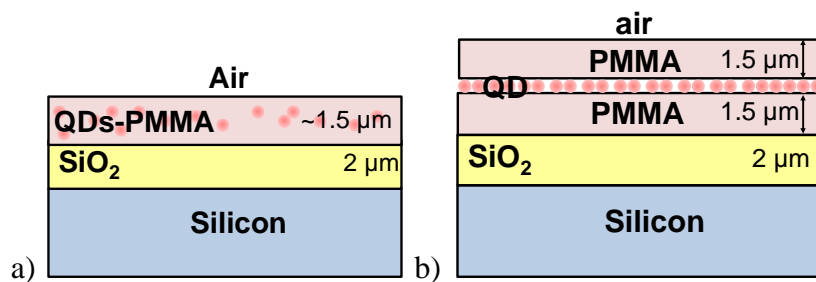


Figure 4- 6: Waveguide structures studied: a) HgTe QDs dispersed homogeneously in a PMMA film and b) a dense close-packed HgTe QD layer sandwiched between two PMMA films. In both cases the polymers are deposited onto a SiO_2/Si substrate.

In a qualitative comparison between HgTe-PMMA (new QD-material) and PbS-PMMA (previous QD-material) waveguides (structures in Figure 4- 6a) we can say that the waveguided photoluminescence intensity is much more important in the first case. However, the initial gain (before saturation) deduced from experiments (Figure 4- 7a) was smaller (250 cm^{-1} as compared to 350 cm^{-1} in PbS/CdS nanostructures, for example). Concerning the losses (Figure 4- 7b), both QD-materials gave similar values, due to the fact that they exhibit similar large Stokes-shift and hence losses are presumably dominated by roughness scattering and not by reabsorption. Moreover, to obtain such values of gain it is necessary to use a high concentration of QDs in the polymer. However, such a high concentrations restricts the propagation of the pump beam through the waveguide due to the strong absorption of the nanocrystals, being it necessary to pump the waveguides from the surface where the pump power density is much lower. Thus, in order to improve the propagation of the pump beam and the generation of photoluminescence the second structure in Figure 4- 6b was proposed. This structure is based on the propagation of the pump laser (400 / 533 nm, particularly) through the PMMA cladding layers, where absorption from pump beam is absent, and a high amount of photoluminescence is generated at the high dense QD-film that is waveguided through the structure. Samples were examined under CW and pulsed laser pumping conditions; in the second case a broader PL spectra (Figure 4- 8), but a faster saturation is observed as compared to the first case. Moreover, HgTe-PMMA waveguide is characterized by a PL spectrum that broadens towards the high energy side by increasing the laser pumping power. This

behavior can be tentatively attributed to multiexcitonic states or a complex excitonic ground state structure.

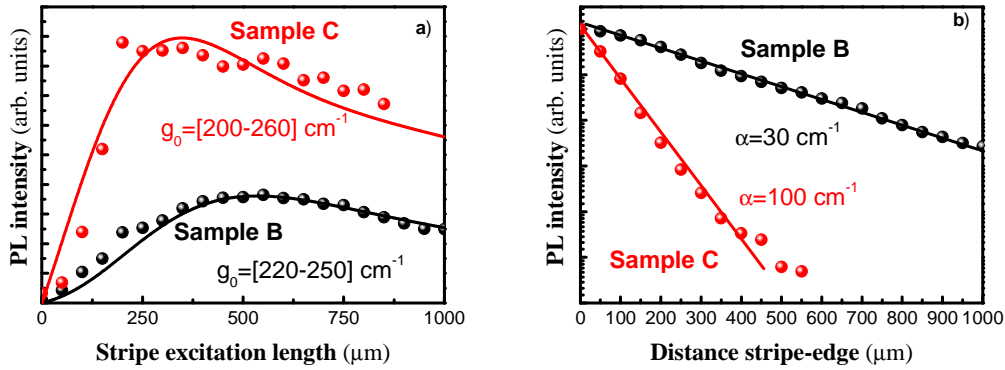


Figure 4- 7: Peak photoluminescence (around 1000 nm) intensity as a function of the stripe excitation length (a, gain) and as a function of the distance between the stripe and the edge of the sample (b, losses). Samples A and B corresponds to QD filling factors of 0.008 and 0.08, respectively.

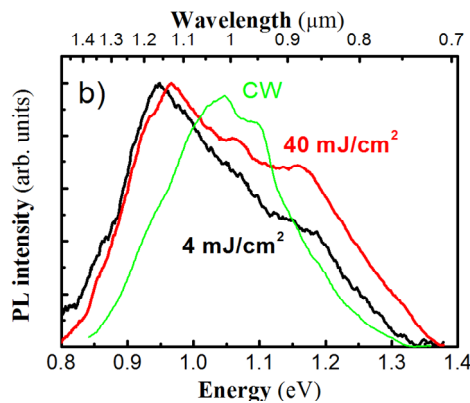


Figure 4- 8: Normalized photoluminescence spectra for two different pulsed pump energies (red and black lines) by using a doubled Nd:Yag at 533 nm in comparison to the case of CW pumping at 405 nm (green line).

To conclude, HgTe QDs seem to be a promising material for active purposes since it exhibits a large Stokes shift and dielectric waveguides exhibit a high amount of waveguided photoluminescence. Although dropped-casting QD layers seem to be unstable with temperature and illumination time, the photostability is rather high once QDs are incorporated into PMMA. However, we do not observe any clear amplification effect in the dielectric waveguides prepared and studied, that is, still presenting gain saturation effects as measured with other previous QD materials. We propose to continue working on HgTe QDs by improving the excitation conditions in order to enhance the pump efficiency and, in parallel, investigate the increase of the surface plasmon polariton propagation length in QD-plasmonic structures, after preliminary positive results achieved at visible wavelengths in test structures, as described below.

Task 4.4 Fabrication and characterization of QD-based plasmonic amplifiers

a) Polymer based version

In the last months we have focus our work in developing plasmonic structures and a direct measure of the propagation length of the surface plasmon polariton (SPP) modes that we can generate on them. Figure 9a corresponds to gold stripes (4 - 20 μm wide) 30 nm thick defined by a lift-off process onto a SiO_2/Si substrate and cladded by a QD-PMMA dielectric active waveguide (1 μm thick in order to avoid high order TM modes). Although this kind of waveguide optimizes the study of the SPP it does not allow the propagation of the pump beam by end-fire coupling, the most optimized optical pumping of QDs inside the polymer as it has been explained above. Nevertheless, this efficient pumping is only possible through a waveguide structure as the one depicted in Figure 9b, which consists of a thin layer 250 nm (close to the evanescent tail of the LR-SPP, as it was explained in deliverable 4.1) thick of the QD-PMMA nanocomposite deposited onto the gold film (30 nm thick) and a PMMA cladding free of QDs. In this way the long range SPP (LR-SPP) mode can be excited optimally, but the propagation of the pump beam is possible without absorption losses. The tests were carried out by using QDs with emission in the visible, given the easier fabrication and characterization as compared to near infrared wavelength (also limited by available materials).

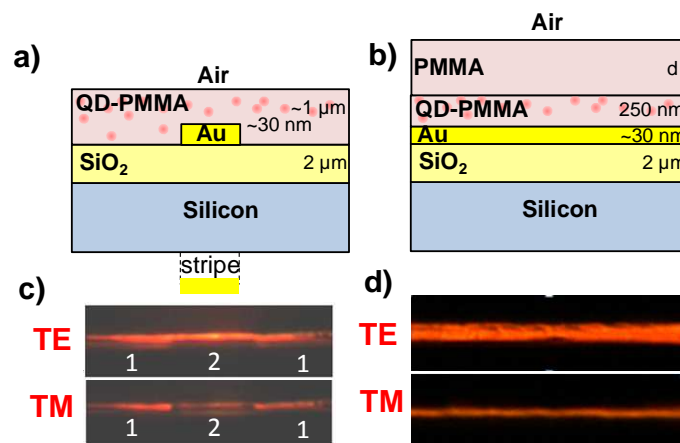


Figure 4- 9: Two plasmonic structures proposed and fabricated for the measurement of the SPP propagation length: Au stripe surrounded by a CdSe-PMMA nanocomposite (a) and double layer nanocomposite plus a thick polymer layers deposited on a Au film. In (c) and (d) the near field characterization of TE and TM optical modes in structures (a) and (b), respectively.

We have developed a novel experimental method that can be used not only to generate a SPP, but also to determine its propagation length and characterize the optical modes of the metal/dielectric plasmonic structure (Figure 4- 9c-d). The SPP is locally generated (at a certain distance from the Au-waveguide edge) through the coupling of the QD photoluminescence into the TM mode of the plasmonic structure by a laser wavelength (**laser probe/signal**: 533 nm) slightly shorter than that corresponding to the QD effective bandgap (around 600 nm); the local excitation is made by using an optical fiber tip, as depicted in Figure 4- 10a. In this way, amplification or propagation length compensation can be easily determined if a laser wavelength (**laser pump**: 405 nm in our experiment) well beyond the QD bandgap is used to pump their photoluminescence uniformly in the plasmonic structure.

Figure 10b shows the photoluminescence integrated intensity excited by the fiber tip as a function of the distance between the tip and the edge of the sample in the plasmonic structure shown in Figure 4- 9a. The curves in TE and TM polarizations exhibit two different decays, given that analyzed light comes from the metal stripe and polymer (see Figure 4- 9a-c). For a distance larger than 50 μm the curves tend to a slow decay corresponding to the photonic mode out of the metal stripe, and it is similar in TE (blue curve) and TM (red curve) polarizations; the first decay ($x < 50 \mu\text{m}$) is much faster in TM because light is centered in the metal for this polarization (the SPP mode). Indeed, the propagation length deduced for the LR-SPP mode is 12.7 μm , very close to the theoretical value (11.7 μm).

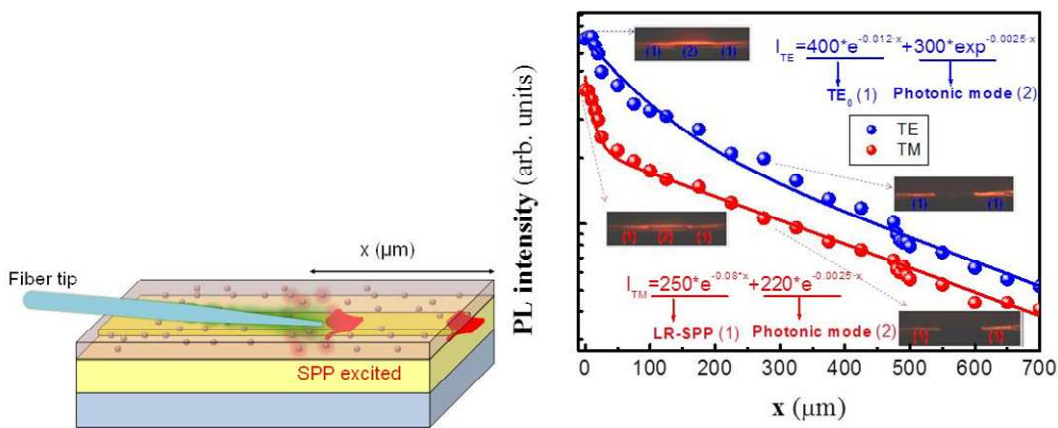


Figure 4- 10: (a) Experimental set-up to characterize the waveguides: coupling light from a fiber tip to the plasmonic structure and analyze the signal as a function of the distance between the fiber and the edge of the sample (x). Propagation length estimation in TE (red) and TM (blue). PL intensity as a function of the distance between the fiber tip and the edge of the sample. Symbols correspond with experimental points and lines to the simulation. Panels plots near field characterization at $x=0$ (modes in and out of the stripe) and $x=250 \mu\text{m}$ (mode out of the stripe).

The same method is applied to the plasmonic structure depicted in Figure 4- 9b. This structure allows the end-fire coupling of the pump laser (405 nm) and hence a uniform and optimized generation of photons at 600 nm (photoluminescence from QDs). Indeed, Figure 4- 9d showed the near field characterization of the waveguided photoluminescence, where the light distribution cross section in TE is wider than the one in TM, because the first mode is centered in the dielectric film (PMMA+nanocomposite) and the second mode in the metal. Figure 4- 11 shows the variation of the photoluminescence integrated intensity as a function of the distance x in TE (Figure 4- 11a) and TM (Figure 4- 11b) polarizations under excitation with the fiber tip (probe laser at 533 nm); the experimental data (symbols) can be fitted by a single exponential decay because the sample is planar and light propagation is dominated by the losses in the gold. In TM the value deduced for the propagation length, L_p , is that found for the LR-SPP from simulations ($L_p = 11.7 \mu\text{m}$). When the pump laser beam (405 nm) is coupled to the input edge of the sample (pump+probe) the decay in both polarizations becomes slower implying an effective increase of L_p by 30 to 45 % in TE and TM modes, respectively. These experiments make us confident to obtain similar results when using plasmonic structures with a QD-polymer material emitting around 1550 nm. As a conclusion of this preliminary study, our next steps will be the fabrication of 1D Au-waveguides by e-beam lithography cladded by double QD-PMMA/PMMA (QDs emitting at infrared wavelengths) layers to prove the increase of the LR-SPP propagation length.

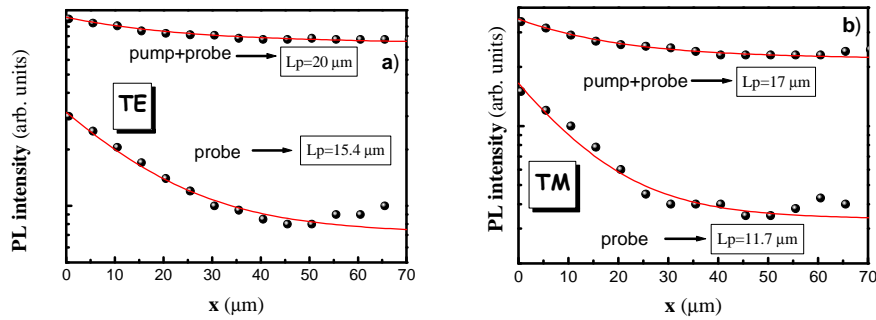


Figure 4- 11: Loss compensation estimation in TE (a) and TM (b). PL intensity as a function of the distance between the fiber tip and the edge of the sample. Symbols correspond with experimental points and lines to the simulation. Conditions under probe and pump+probe excitations are indicated.

b) Hybrid silicon version

While waiting for the optimized QDs we improved the process for depositing QDs at a dedicated location on the wafer (e.g. within a laser or amplifier cavity). We developed a process combining lift-off lithography (with optimized lift-off procedure) and Langmuir-Blodgett deposition that now allows us to define areas with QDs with sub-micrometer dimensions and +/- 150nm alignment accuracy. The pictures in Figure 4- 12 show some examples.

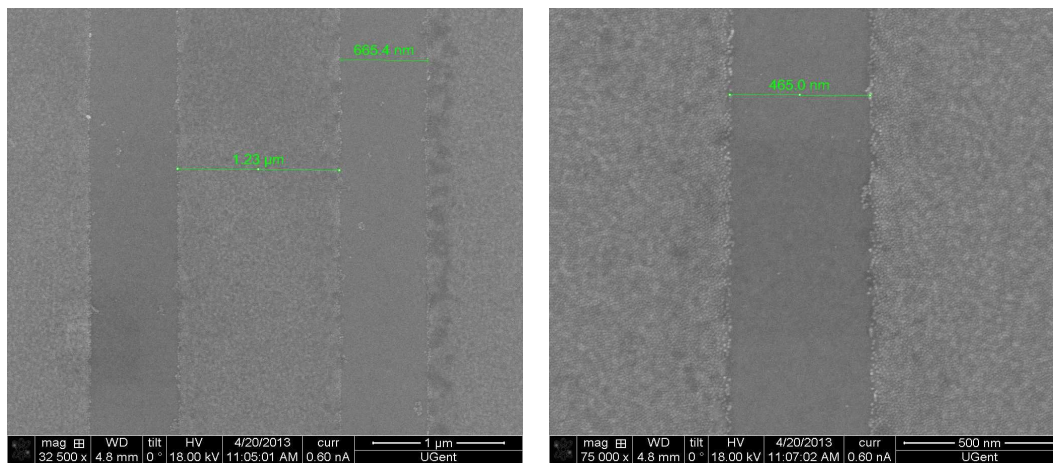


Figure 4- 12: QD-patterns defined using optimized lift-off procedure.

Task 4.5 Fabrication of plasmonic polymer QD based photodetectors

In the last months we have optimized the synthesis of PbS QDs emitting at wavelengths around 1550 nm, as observed in Figure 4- 13. Simultaneously, we have prepared QD thin films around 300-400 nm thick by means of a dr. Blading deposition technique in order to decrease the effect of granularity/roughness obtained until now by spin-coating that was limiting, presumably, the I(V) and responsivity of photoconductors/photodetectors prepared by this method. More details can be found in MS23. In parallel, but as a secondary activity, the use of other ligands for the layer-by-layer method and synthesis of alternative QD materials were initiated with the aim to obtain Pb-free and more stable QD films. We have continued producing PbS QD films on glass (for micro-gap photoconductors) and glass/ITO/PEDOT (for Schottky/heterostructure photovoltaic photodetectors)

substrates. These layers and devices maintain their good electro-optical properties (shown below) stable in air for more than 2 months.

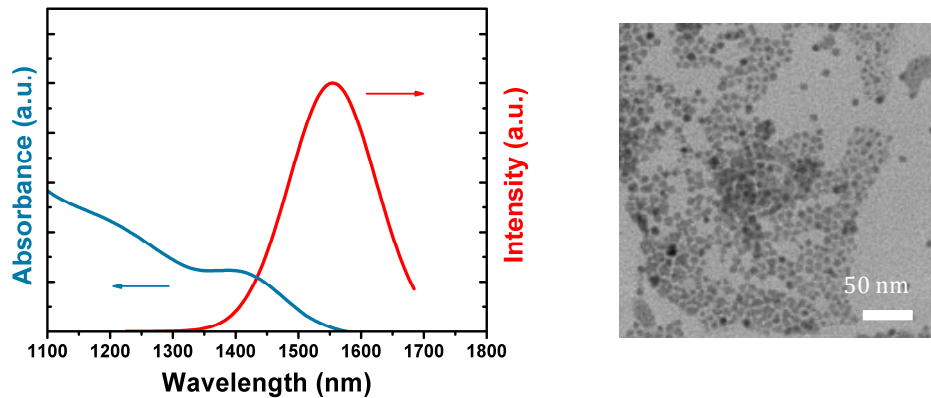


Figure 4- 13: Absorption and photoluminescence spectra (left) and TEM image (right) of oleyamine-capped PbS QDs in octane.

Figure 4- 14 shows the comparison of the I(V) characteristics under dark and illumination (800/820 nm) for two Schottky photodiodes, one from the old series where the QD-film was prepared by spin coating (left plot) and one from the new series where the QD-film was prepared by dr. Blading (right plot). First of all, it should be noted the reduction of reverse current under darkness and the big increase by more than a factor ten observed in the open circuit voltage (V_{OC}) under illumination; this improvement in V_{OC} is attributed to the new deposition technique leading to a smoother film surface (reduction of the film granularity) and hence reducing the series resistance limitation, as predicted in our previous report. The photocurrent is very similar, but this is an apparent value, because the incident power was slightly different in both measurements and the QD-film would a different absorption coefficient at 800 nm for the new device series (whose I(V) is shown in the right plot of Figure 4- 14), given that the size of the PbS QDs (emission at around 1550 nm, as shown in Figure 4- 13) is bigger than in previous series (emission at around 1000 nm, as previously reported). These differences are included in the responsivity measured in the new series (0.04 A/W) that turns to be enhanced by a factor ten as compared to the old ones.

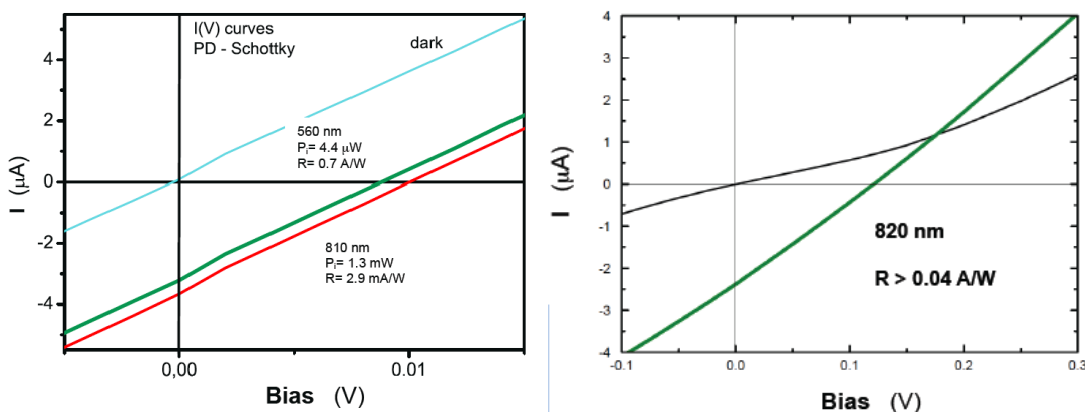


Figure 4- 14: Comparison of the I(V) characteristics of the best ITO/PDOT/PbS-QD-solid/Ag photodiodes: spin-coating (left, from previous report) and DrBlade (right). The QD-film thickness is very similar in both devices (360 and 300 nm).

The measurement of the responsivity at longer wavelengths has been recently accomplished by the new characterization set-up that includes a Ge calibrated photodiode. The excitation source is an halogen lamp coupled into the monochromator (300 g/mm, blaze at 1500 nm) through an optical fiber. The power at the exit of the monochromator is of the order of 100 nW/nm and the electrical signal of the QD(PbS)-based photodetector was amplified by a factor 10^8 using a trans-impedance amplifier. Figure 4- 15 shows the responsivity curve of the QD(PbS)-based Schottky photodiode after taking into account the transmission of the glass+ITO+PDOT and a second glass used as the device holder through which light propagates before reaching the QD-film (this correction was not considered in previous measurements, as the one shown in Figure 4- 14). We can observe a nearly maximum response in this spectral region of around 0.095 A/W at 1200 nm and a smooth decrease from 1200 to 1500 nm, where the responsivity value is around 0.08 A/W. Beyond 1500 nm the responsivity drops faster (0.042 A/W at 1670 nm), which is consistent with the observed absorbance and photoluminescence spectra of the colloid (Figure 4- 13), given that the QD(PbS)-film is relatively thin (300 nm) and light scattering by surface roughness is possibly smearing its absorbance spectrum (blue line in Figure 4- 15). At wavelengths below 1000 nm (not shown here) the responsivity increases up to values around 0.15 A/W.

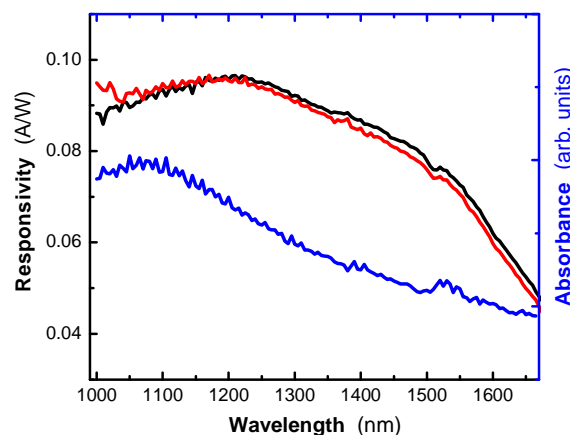


Figure 4- 15: Responsivity spectra (left) and absorption (right) measured in two different glass/ITO/PEDOT/QD-film/Ag photodiodes of the same sample.

The present results are demonstrating that the use of PbS QDs deposited by a solution processing technique on a glass-ITO substrate can be the basis to fabricate reasonably good Schottky photodiodes exhibiting responsivities larger than 0.1 A/W at telecom wavelengths (target in NAVOLCHI project), for the moment very close to this value with the use of the most simple device. The Schottky concept is a very convenient device to be integrated in SOI technology, because photocurrent or photovoltage can be directly measured without needing polarization. As next steps we will try to improve this photodevice by means of: i) increasing the QD-film thickness, ii) using plasmonic scatterers as a substitute of an antireflective coating, iii) using more effective ligands for reducing surface trap levels, and iv) trying other top metal electrodes. In parallel, microgap and nanogap photoconductors are under processing at the moment.

Status deliverables and milestones

MS22 and MS3 have been prepared and submitted.

MS22	Demonstration of plasmonic amplifiers with optical pumping exhibiting 10dB gain	4	IMEC	21	07/2013
MS23	Operation of QD based photodetector with responsivity > 0.1 A/W	4	UVEG	24	10/2013
MS24	Demonstration of SPP amplifiers with electrical injection exhibiting 10dB/cm gain	4	UVEG	30	01/2014

Next deliverables:

D4.4	Report on SPP amplifiers by using QDs	4	IMCV	30	4/2014
D4.5	Report on plasmonic photodetectors	4	UVEG	33	9/2014

3.2.5 Work Package 5: Optical and Electrical Interfaces

Task 5.1 Modelling and fabrication of coupling Si waveguide to plasmonic waveguide

Tapered Couplers: The tapered couplers are numerically optimized, fabricated and tested. The mode converters have been fabricated as a part of plasmonic modulators. The modulators with various device lengths and with a slot size of 140 nm and 200 nm are fabricated on silicon on insulator (SOI) platform, where the silicon nanowire waveguides are used as access waveguides. The fabrication procedure is described in Milestone 11, “Fabrication of plasmonic modulator on a SOI platform” and Deliverable 3.4, “Report on fabrication of modulators”. Optical and scanning electron microscope images of the first generation device with device length of 34 μm and the slot size of 200 nm are given in Figure 5- 1(a) and Figure 5- 1(b), respectively.

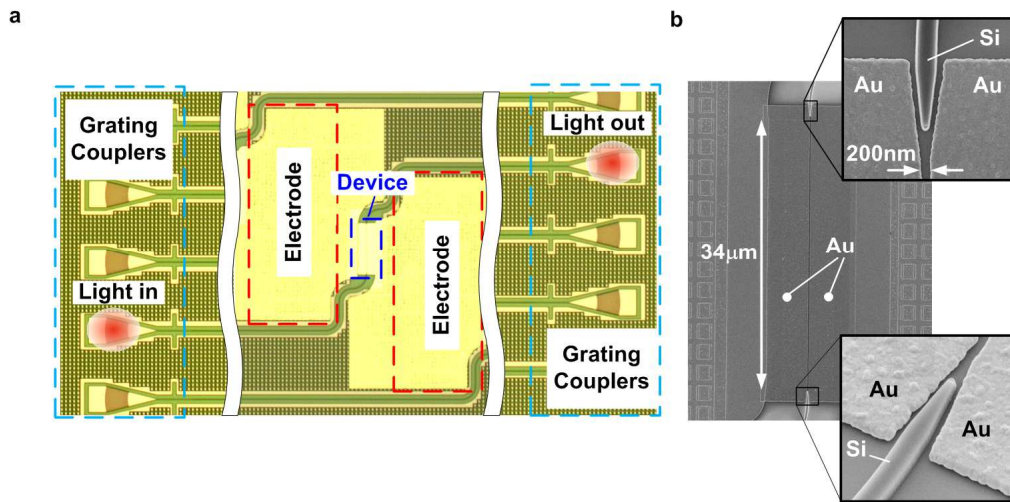


Figure 5- 1: Fabricated plasmonic phase modulator on silicon on insulator platform. (a) Optical microscope image of the device. Silicon nanowire waveguides are used as access waveguides for the plasmonic modulator. Light is launched in and out from the chip using grating couplers. (b) Scanning electron microscope image of the modulator with a length of 34 μm and a slot size of 200 nm. Metallic tapers are used for photonic to plasmonic mode conversion.

We used the experimental setup given in Figure 5- 2 for passive optical characterization. Light with from a tuneable laser source (TLS) is coupled into the device using a single mode fibers and a diffraction grating coupler. The transmitted optical power at the output of the device is measured with optical spectrum analyzer (OSA). We measured the optical loss of the modulator section by taking an equal-length of SOI strip waveguide as a reference. Example of the transmission spectrum of 34 μm long plasmonic modulator with a slot size of 200 nm is given in Figure 5- 2. The average total loss is 12 dB (black solid line), close to the theoretically expected value (blue dashed horizontal line).

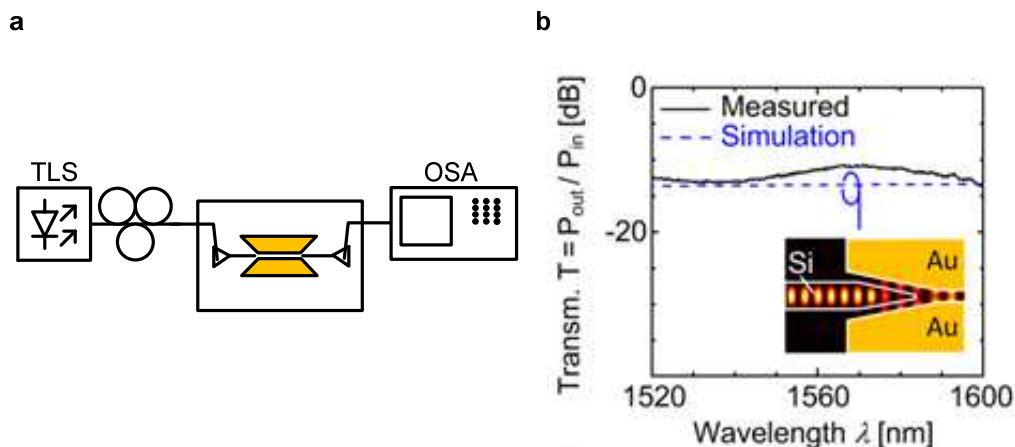


Figure 5- 2: The experimental setup used for passive optical characterization and the transmission spectrum of the plasmonic phase modulators. (a) The experimental setup used for measuring the optical losses of the device. Light from the tuneable laser source (TLS) is launched into the chip and the transmission spectrum is measured at the output using optical spectrum analyser (OSA). (b) The transmission spectrum of the 34 μm long device with a slot size of 200 nm, black solid line. The theoretically expected transmission spectrum is given in the blue dashed line.

We have performed an SPP coupling loss estimation on our second generation of plasmonic modulators with a slot size of 140 nm. A good alignment and a desired 140 nm slot size have been achieved for the modulators with a length of 1 μm , 29 μm and 44 μm . We used the measured losses at the wavelength of 1550 nm to derive the propagation loss and the coupling loss of our modulators. By fitting the total loss versus device length dependence with a linear function we could estimate that the coupling loss and the propagation loss at 1550 nm wavelength, see Figure 5-3. The coupling loss in our second generation device is reduced below 1 dB. The propagation loss in the modulator with a slot size of 140 nm is 0.52dB / μm which is very close to theoretically expected value of 0.48dB / μm .

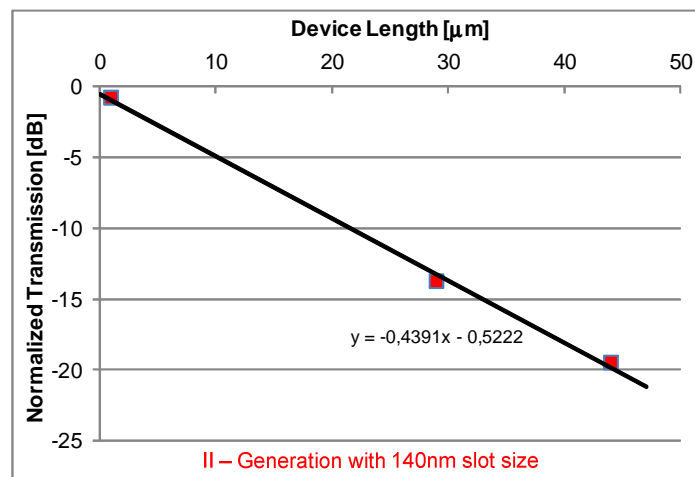


Figure 5- 3: Measured power transmission at the wavelength of 1550nm for plasmonic modulators with various lengths. Performing linear fit we can estimate the SPP coupling and propagation losses in the modulator.

Side Couplers: Horizontal metallic slot waveguide can be excited with a directional coupler configuration. In this coupling scheme, the photonic mode propagating through the silicon nanowire is phase matched with the SPP in a horizontal slot waveguide. SPP is then excited with the photonic mode propagating through the silicon nanowire similar to the conventional multimode interference couplers, see Figure 5- 2.

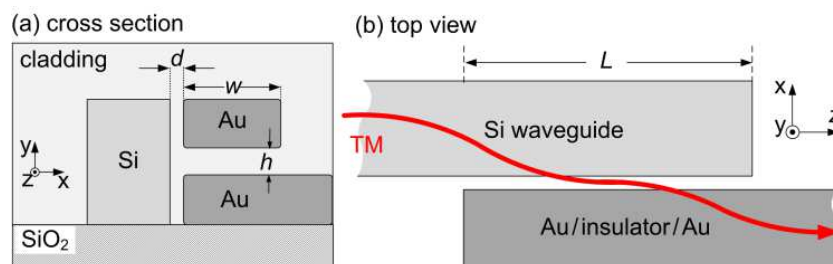


Figure 5- 4: (a) Cross section and (b) top view of the suggested coupler. The TM mode launched into the silicon nanowire couples to a plasmonic waveguide via a coupling section of length L.

We extended our previous study of this kind of plasmonic couplers and the results now have been reported in the Deliverable 5.5 “Report on plasmonic couplers”. In the Figure 5- 5, the conversion efficiency and the coupling length as a function of the distance d and the slot

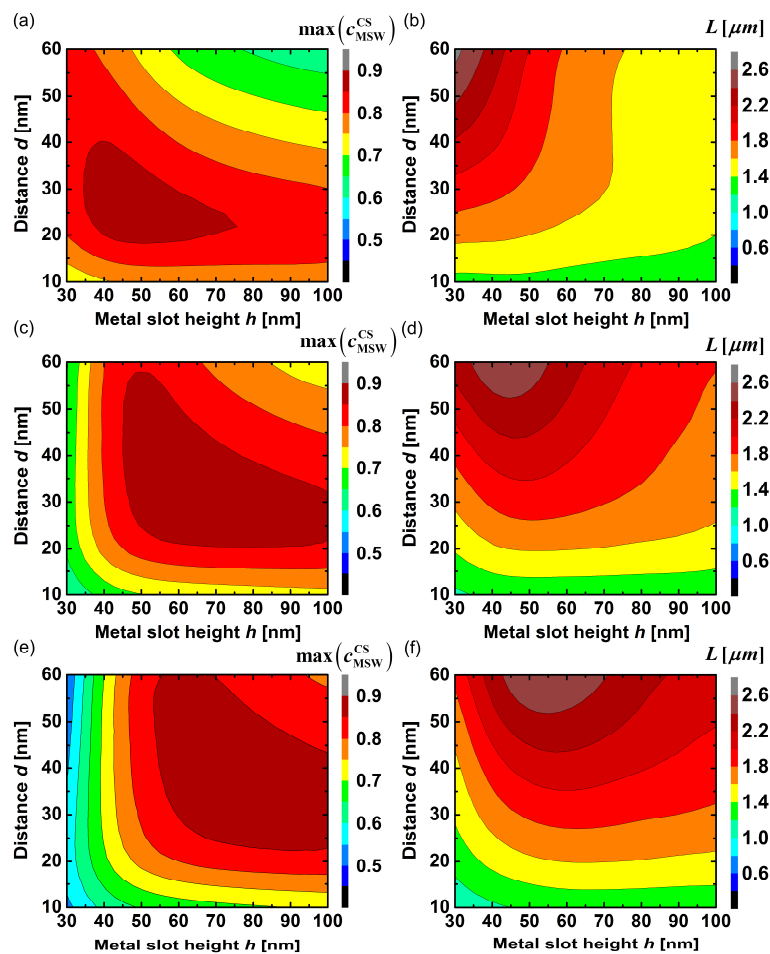


Figure 5- 5: Conversion efficiency Fehler! Es ist nicht möglich, durch die Bearbeitung von Feldfunktionen Objekte zu erstellen. (a), (c), (e) and optimum CS length L (b), (d), (f) for a MSW with a width w of 200 nm and for various cladding materials: (a) and (b) for Glass, (c) and (d) for organic materials with refractive indices of 1.6 and (e) and (f) for refractive index of 1.7.

are given for MSWs with a width w of 200 nm for various cladding materials. Glass with a refractive index of 1.44, see Figure 5- 5 (a), (b), and organic materials with refractive indices of 1.6, see Figure 5- 5 (c), (d), and 1.7, see Figure 5- 5 (e), (f), are considered as cladding materials. For all three types of cladding materials, conversion efficiencies exceeding 85 % can be achieved for MSWs with sub - 50nm slots. Moreover, by varying geometrical parameters e.g. the distance d , the conversion efficiency can be tuned. This might be needed e. g. in the case of plasmonic coupling scheme shows a great tolerance to fabrication errors in defining the length L .

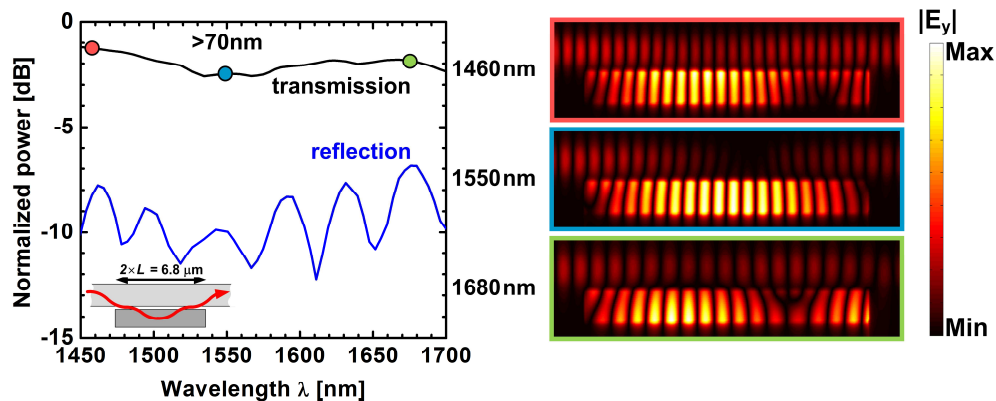


Figure 5- 6: Transmission and reflection spectra in the converter with a height h of 30 nm, a distance d of 60 nm and a cladding material with a refractive index of 1.44. The dip in the transmission shows the good photonic / plasmonic mode conversion, in which case the Ohmic losses are the highest. In addition, the electric field distributions for three different carrier wavelengths are given in the right side. It can be seen that the photonic mode is fully converted in a gap SPP in the case of 1550 nm wavelength.

To investigate how the performance of the proposed mode converter depends on the operating carrier wavelength, we investigate the mode conversion mechanism in a converter with a silicon dioxide cladding by finite difference time domain (FDTD) method simulations. In this particular simulation a metallic slot height h of 30 nm and a distance d of 60 nm have been chosen. A continuous silicon nanowire is used with a CS length of $2 \times L$ of 6.8 μm , as plotted in the inset of Figure 5- 6. Transmission and reflection spectra are given in Figure 5- 6. The wavelength dependence of the optical properties of Au is taken into account by the Drude model. No strong resonance behaviour is seen in the optical response of the mode converter. The operating wavelength range of the proposed device is in the range of 50 nm, which is comparable to the one reported for metallic taper mode converters.

Task 5.2 Design and fabrication of Si beam shaper

In the first half of the project we focused on electrostatically moved grating couplers. For the second generation we will focus on the design of grating couplers allowing to couple a transmitter and receiver chip through free space over distances from 0.1 to 1.0 mm. This work started with a high level design study, estimating the distance that can be expected and the form factor of the grating that should be used. The pictures below summarize these results. These figures show the different tradeoffs involved. For coupling over short distances it is better to use small grating couplers, which allow a reduced device pitch and broader wavelength operation (smaller gratings = stronger grating with less periods = broadband operation). However, these gratings have stronger diffraction and if coupling over larger distances is needed the size of the grating has to be increased to reduce diffraction and keep the device to device pitch minimal. However, the device to device pitch increases (along the black line for in figures below, for optimized case) and the optical bandwidth decreases.

Based on these results we are now starting to design gratings aimed at coupling over distance of 0.1, 0.5 and 1.0mm total distance. These will be implemented in the standard SOI platform in the coming months, both in a standard way (Figure 5- 7) and as focusing gratings (Figure 5- 8). In the latter case the chip to chip distance can be doubled but the alignment tolerance is roughly halved.

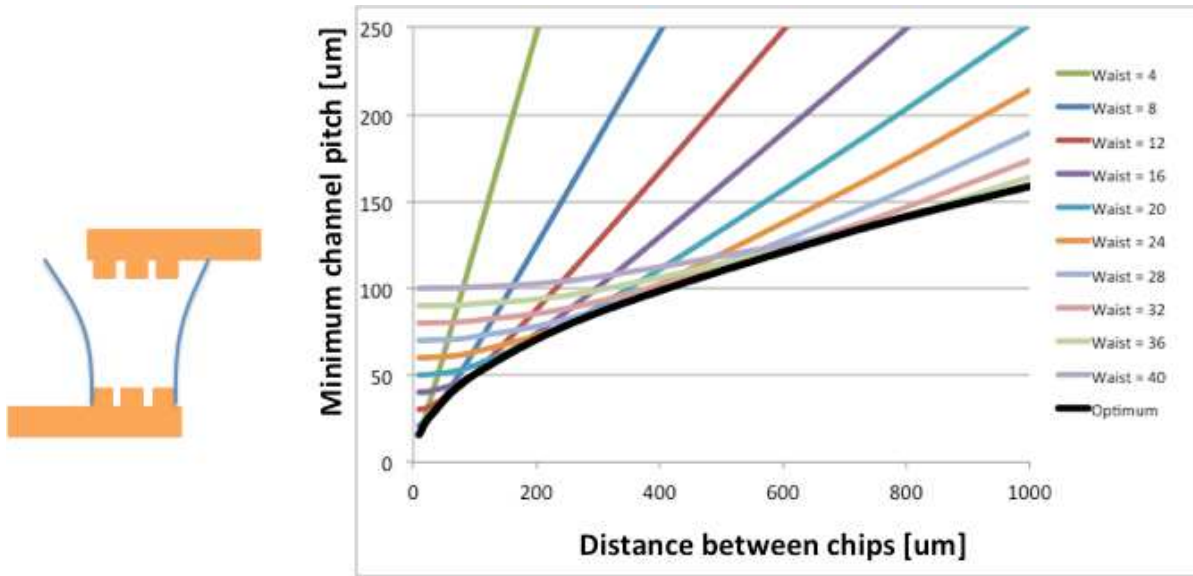


Figure 5- 7: Minimum channel pitch as function of distance between chips for different initial grating sizes (grating size equal to beam waist)

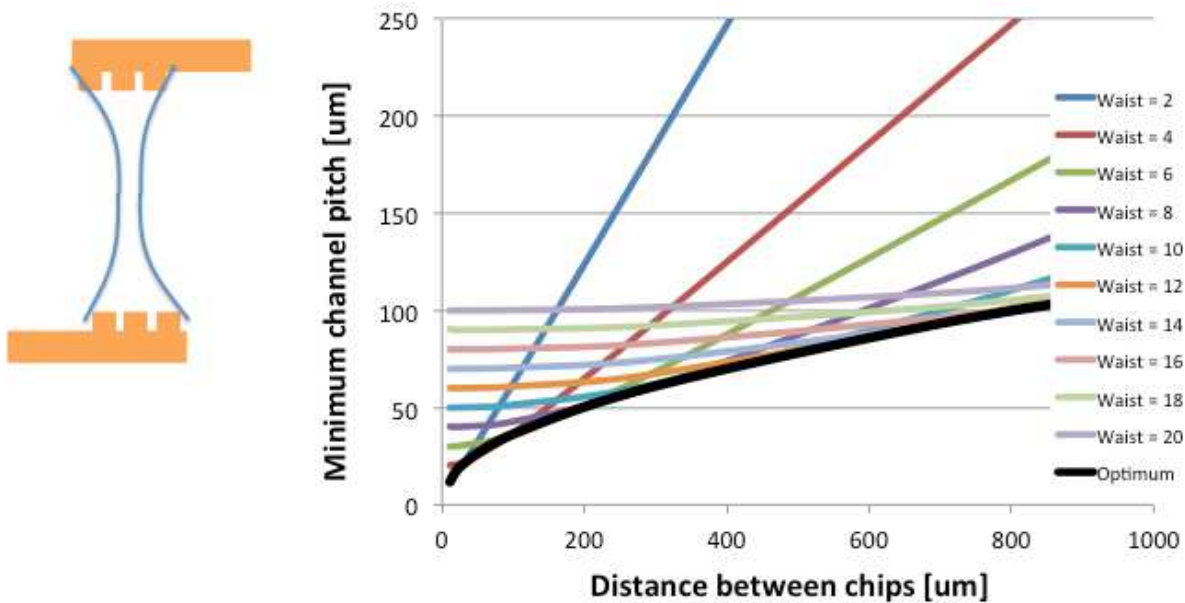


Figure 5- 8: Minimum channel pitch as function of distance between chips for different initial grating sizes (focusing gratings)

Task 5.3 Design and fabrication of passive ultra-compact components as filters

This task was finished during the previous reporting period (see D5.3 for details)

Task 5.4 Signal generation module design

The signal generation module, called DDCM (Dual Dice Communication Module) has been specified and implemented in VHDL, synthesized and characterized in terms of area and timing last year.

The subsequent step was to replace the previous PHY adapter, suitable for a “classical” electrical chip to chip communication, with the new PHY adapter exploiting the VHDL components developed in WP2 (bi-synchronous FIFOs, serializer, deserializer, Bus Inverter and Optical Bus Inverter encoders and decoders, Clock Recovery Circuit), suitable for supporting a physical layer exploiting plasmonic components.

This “integration” activity has been carried out in December 2013 and January 2014 and two DDCM modules with the new PHY adapter have been verified back to back.

Task 5.5 Signal Generation Module implementation via FPGA

FPGA mapping activity has been impacted by some HW failures and some problems with SW licenses. It started actually in January 2014, and in order to speed up the process at first a simplified system, composed of only a PHY adapter transmitter and a PHY adapter receiver connected back to back will be implemented. This in any case is sufficient to effectively test the off-chip plasmonic interconnect. In a second phase, if enough time is available, the whole system including two complete DDCM modules will be implemented.

In both cases at first the system will include classical electrical PHY (wires) implementing the chip to chip communication. Then the electrical PHY will be replaced with the novel PHY exploiting plasmonic components, that will be available as discrete components mounted on small boards driven by the digital parts mapped onto FPGA.

Because of an objective difficulty in moving ST FPGA equipment from Catania (it’s embedded within a server shared with other ST groups requiring to work with it) it has been agreed that the synthesized rtl, after all the verifications have been run, will be sent to another partner responsible for mapping it onto an own FPGA that will be easily interfaced with the board where the plasmonic interconnect components will be integrated.

Deliverables in third reporting period (month 19 – month 27)

D5.3 - Compact optical filters (2nm bandwidth, >30nm FSR) and first generation beam shapers (month 21) → Completed

D5.4 - Generic DDCM compatible with plasmonic-based PHY specification document (month 24) → Completed

D5.5 – Report on plasmonic couplers → Completed

Upcoming deliverables:

D5.6 - Generic DDCM compatible with plasmonic-based PHY design and verification data base (month 30) → No delay expected

D5.7 - Second generation beam shapers (distance 1mm, with bandwidth > 10nm and efficiency > 3dB) (month 33) → Delay till month 33

Milestones in third reporting period (month 19- month 27)

MS33 - Design of second generation beam shapers (month 24) → Delayed till March 2014

MS34 - Generic DDCM compatible with plasmonic-based PHY (month 24) → Completed

Upcoming milestones

MS35 - Fabrication of compact optical filters and first generation beam shapers (month 30) → Delay till month 32

MS36 - DDCM evolution for NiP solutions (month 30) → No delay expected

3.2.6 Work Package 6: Integration, Characterising and Testing

Task 6.1 Characterization of active and plasmonic devices

Two generations of plasmonic phase modulators (PPMs) are fabricated on the SOI platform [1]. The first generation (1stG) of PPM has been fabricated in a ground-signal-ground (GSG) configuration with metallic slots with a length of $34\ \mu\text{m}$ and a slot width of $200\ \text{nm}$. In the second generation (2ndG) PPM, the slot size has been reduced down to $140\ \text{nm}$, and the length was reduced to $29\ \mu\text{m}$. The fabricated PPMs show broadband optical transmission with an average total loss of $12\ \text{dB}$, see Figure 6- 1(b) [1]. We also measured the capacitance of the metallic slots to be $C_{1\text{stG}} \approx 2.2\ \text{fF}$ and $C_{2\text{ndG}} \approx 2.7\ \text{fF}$ for first and second generation devices, respectively [1].

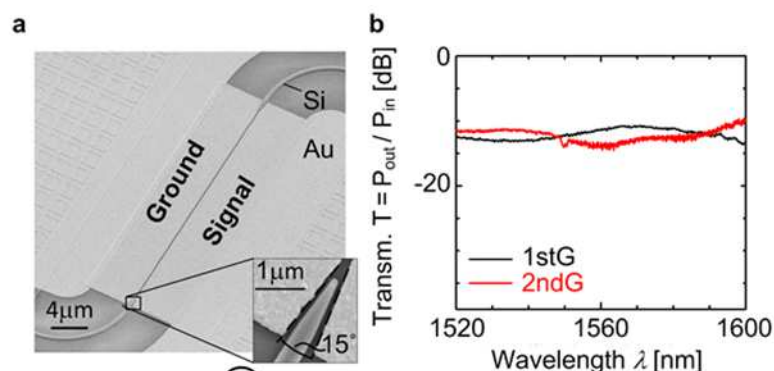


Figure 6- 1: (a) Scanning electron microscope (SEM) picture of the 1stG plasmonic phase modulator with a length of $34\ \mu\text{m}$. (b) Comparison of the measured optical transmission of the 1stG device (black solid curve) with 2ndG modulators (red solid line) after coated with an electro-optic polymer. A flat transmission across a wide spectral range is seen [1].

We characterized the electro-optic frequency response of the modulators using the measurement setup given in the inset of a Figure 6- 2(a). The modulators are driven with a sinusoidal RF signal

with an amplitude of U_m and the resulting modulation index is measured. The measured phase modulation index for the 2ndG modulator is shown in Figure 2(a) as a function of the RF modulation frequency up to 65 GHz. To cover the entire RF frequency range of the driver we have selected relatively small driving voltage amplitude of $U_m = 0.1$ V. The device exhibits an ultra-flat frequency response up to at least 65 GHz. The optical response is measure to be flat across 120nm wavelength range, see Figure 6- 2(b). The electro-optic coefficients obtained in 1stG and 2ndG devices to be $r_{33} = 13$ pm / V and $r_{33} = 21$ pm / V, respectively.

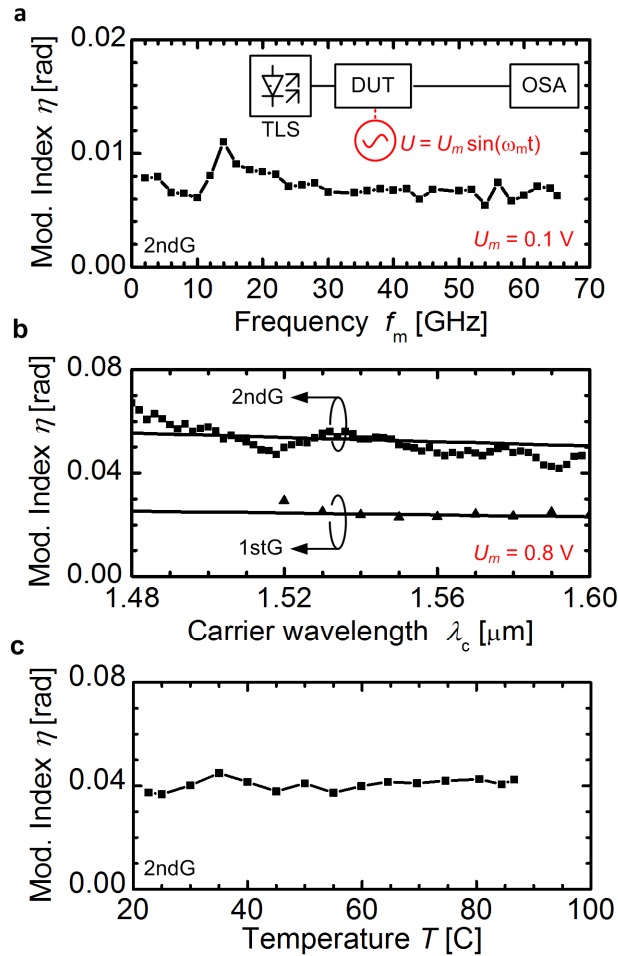


Figure 6- 2: (a) Modulation index η versus RF frequency f_m for 2ndG modulator. The frequency response is flat up to 65 GHz. Experimental setup used for measuring the phase modulation index η is given as an inset. (b) Modulation index for 1stG and 2ndG modulator versus optical carrier wavelength in a range of 120 nm for a modulation frequency of $f_m = 45$ GHz. The modulation index is flat with respect to the carrier wavelength in a range of 120 nm [1].

Even though the used nonlinear polymer has been previously tested in a high temperature environment [2], we tested the thermal stability of our plasmonic phase modulators. The modulation index has been measured for various sample temperatures up to 85° C. No degradation of the modulation index has been found, see Figure 6- 2(c).

To test the high-speed capabilities of the 2stG modulator we encode a data stream with a bit rate of up to 40 Gbit/s. The phase of the SPP is encoded with a $2^{31} - 1$ long pseudo-random bit sequence (PRBS) at a voltage swing of $U_{pp} = 4.7$ V, resulting in a peak-to-peak phase modulation of 0.31 rad.

This signal was subsequently converted into an intensity modulated signal by means of a delay interferometer (DI) with a free spectral range (FSR) of 40 GHz, see Figure 6- 3(a). The signal is then directly detected with a single photodiode. A measured eye diagram with a BER of 6×10^{-5} is given in Figure 6- 3(b). Taking into account the capacitance C_{2ndG} of the modulator we estimate an energy consumption per bit of $(2U_{pp})^2 \times C_{2ndG} / 4 = 60$ fJ / bit for a voltage swing $2U_{pp}$ across the device [4].

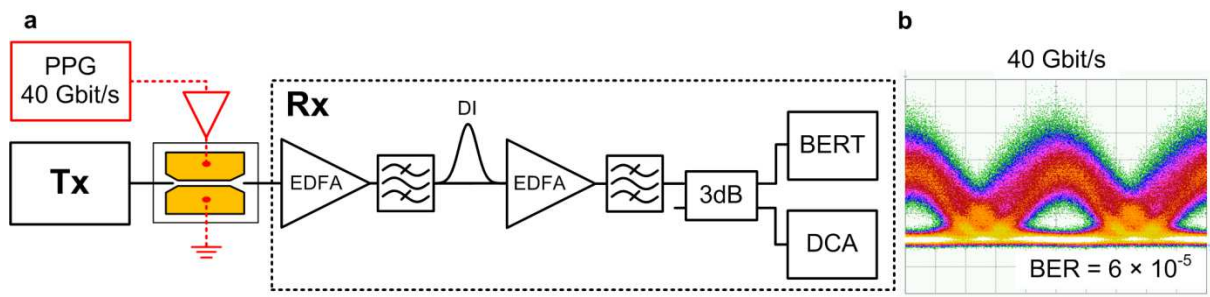


Figure 6- 3: Modulation experiments with the 2ndG plasmonic phase modulator. a Direct receiver setup for detecting a binary phase shift keyed (BPSK) signal. 40 Gbit/s BPSK signal is converted in an intensity modulated signal using a delay interferometer (DI) with a free spectral range of 40 GHz. Digital communication analyser (DCA) and bit error ratio tester (BERT) are taken for eye diagram and BER measurement, respectively. b Eye diagram of the received signal for the data rate of 40 Gbit / s with a corresponding BER of 6×10^{-5} [1].

- [1] A. Melikyan, et al. High-speed plasmonic phase modulators. *Nat. Photon.*, Advance online publication. doi:10.1038/nphoton.2014.9 <http://dx.doi.org/10.1038/nphoton.2014.9>
- [2] Jin, D. et al. EO polymer modulators reliability study. *Proc. SPIE 7599, Organic Photonic Materials and Devices XII*, (2010).
- [3] Schmogrow, R. et al. Error vector magnitude as a performance measure for advanced modulation formats. *IEEE Photonic. Tech. L.* **24**, 61–63 (2012). Correction: *ibid.* **24**, 2198 (2012).
- [4] Miller, D. A. B. Energy consumption in optical modulators for interconnects. *Opt. Express* **20**, A293–A308 (2012).

Task 6.2 Assembly and packaging of plasmonic devices into System-in-Package

The goal of this task, led by KIT is to integrate plasmonic transmitter and receiver in a unique device, test and characterize it. This task will start in month 30.

Task 6.3 Plasmonic chip to chip interconnect prototype testing and evaluation

This task, led by AIT, aims at integrating plasmonic devices and building a full plasmonic interconnect. This task will start in month 32.

Task 6.4 System-in-Package integration and characterization

The objective of this task is to integrate a simple but complete SiP, exploiting the electronic parts developed by ST and the plasmonic devices developed by the other partners.

As ST declared to reduce its contribution to WP6, this task has to be redistributed, see chapters 3.3.6 and 3.3.7 for more details.

Up to now, the main activity carried out in ST during the first 18 months of the project, linked to the integration of the demonstrator SiP, is the development of a Transaction Level Model (TLM) view of the platform that will be used for the final validation of the system.

This platform, allowing generating the stimuli for the system to be validated, will be used in a first phase for the validation of the RTL VHDL view of the overall system, and in a second phase for the validation of the system mapped onto FPGA.

At first the system will include classical electrical PHY (wires) implementing the chip to chip communication. Then the electrical PHY will be replaced with the novel PHY exploiting plasmonic components, that will be available as discrete components mounted on small boards driven by the digital parts mapped onto FPGA.

Two scenarios have been identified for the integration, demonstration and performance evaluation of the NAVOLCHI system:

In the first scenario the transmitter is based on the direct modulation of metallo-dielectric nanolaser while in the second scenario the transmitter is based on the external laser with a phase/amplitude modulator.

In both cases the collector will be based on IMEC Si/Ge photodetector.

All the cases have been extensively simulated and the performance evaluation of the considered scenarios have been presented in D2.3 “Investigation of chip-to-chip interconnection level specifications employing new plasmonic devices”.

In the following sections we describe the expected interconnect parameters at system level both for the transmitter and the receiver.

Transmitter

a) Direct modulation of metallo-dielectric nanolaser

The direct modulation of the metallo-dielectric nanolaser has been identified as a promising scenario for the project demonstrator. External driving electronics would electrically pump the nanolaser, which will be coupled to a waveguide connected to a grating coupler that sends the signal to the receiver. Such interconnection will be either by optical fibers or free-space. Although promising, this scenario still has several challenges to overcome with respect to the nanolaser fabrication technology.

Parameter	Expected value
-----------	----------------

Wavelength	1.4 – 1.55 μm
Driving Voltage	2V for 40 μW
Current	Threshold current = 120 μA 420 μA (2V) for 40 μW
Device Length	< 1 μm
Output Power	40 μW

Table 1: Parameters for the direct modulation of metallo-dielectric-nanolaser. The values correspond to simulation results, since experimental data are not available yet.

b) External laser with a phase/amplitude modulator

The specifications of the second configuration in which an external laser is used with a phase modulator are shown in the following tables:

Parameter	Expected value
Wavelength	1550nm +- 50 nm.
Driving Voltage	> 1.5 V
Current	> 1 mA (above 3mA at room temperature)
Device Length	> 10 μm
Output Power	up to 13 dBm

Table 2: Parameters for the external laser

Parameter	Targeted Value
Overall loss	< 30 dB
Length	< 50 μm
Latency	> 10 μm
Driving Voltage	$\leq 4.5V_{pp}$

Table 3: Parameters for phase/amplitude modulator

Receiver

The receiver will be based on the IMEC Si/Ge photodetector.

a) Si/Ge Photodetector

The IMEC detector is defined using Ge-selective growth on the silicon waveguides, in a two-step epitaxial process.

Parameter	Targeted Value
Reponsivity	0.4 A/W (on chip), @ 1550nm
Dark Current	<100nA
BW	10GHz

Table 4: Parameters for Si/Ge photodetector.

Concerning the reviewers comments at the review meeting after month 18, particularly

- an overall simulation based on above mentioned values including the new phase modulator presented in a Nature publication by beginning of 2014 (see publications list of chapter 3.2.7), and
- the comparison with commercial data and data from other research groups

we refer to the milestone MS39 document, which will be delivered at end of May 2014.

Deliverables in second reporting period (month 10 – month 27)

D6.1 - Report on characterization results of all plasmonic devices. This part is delayed by 6 months due to several technical reasons. See Section 3.3.7 for detailed explanations of each partner

D6.2 - Report on characterization results of all optical interface plasmonic passive components. This part is delayed as well, see Section 3.3.7 for detailed explanations of each partner

Upcoming deliverables:

D6.3 – DDCM Report on chip to chip interconnect characterization (month 36)

→ A delay of about 3 months is expected, please refer to chapters 3.3.6 and 3.3.7.

D6.4 – Report on plasmonic system-in-package interconnect prototype testing and evaluation (month 36)

→ A delay of about 6 months is expected, please refer to chapters 3.3.6 and 3.3.7.

Milestones in second reporting period (month 10- month 27)

M38 - Plasmonic passive components characterization results with a 1dB coupling loss (month 24)

→ In time

M39 - Concept for system integration developed (month 27)

→ Submitted with delay by end of May 2014

Upcoming milestones

M40 - Individual plasmonic devices characterization, testing and evaluation (month 30)

→ No delay expected so far

MS41 - Chip to chip interconnect characterization (month 33)

→ 3 months of delay is expected

MS42 - Plasmonic components integration to demonstrate chip-to-chip interconnect (month 33)

→ 3 months of delay is expected

MS43 - Plasmonic chip to chip interconnect prototype testing and evaluation (month 36)

→ 6 months of delay is expected

3.2.7 Work Package 7: Exploitation and Dissemination

General Status

During the first half of NAVOLCHI, Task 7.1 (Dissemination) and Task 7.2 (Exploitation) have been officially active, while Task 7.3 (Promotion) started on month 24. NAVOLCHI partners have contributed several publications to high-quality scientific journals, magazines and conferences disseminating project results. Communication has been established with another plasmonics-related EU-funded project (PLATON). The NAVOLCHI consortium is committed to the continuation of the dissemination and exploitation effort.

In the first 18 months of the project, there were three milestones to be met. Two have been met successfully (MS44, MS45), while MS46 is currently delayed. There were 4 deliverables to be submitted (D7.1, D7.2, D7.3, D7.4), and have been submitted successfully.

Task 7.1 Dissemination

Dissemination of ideas and results is of high importance in the NAVOLCHI project. The partners of NAVOLCHI are top research organizations with proven track records in their field and are very active in disseminating research results in a worldwide range to scientists, industry, and the public.

Dissemination activities this far

There has been significant dissemination action concerning NAVOLCHI activities and results. In particular:

- Nine journal and conference publications (talks/papers/abstracts) disseminating the project have been published by NAVOLCHI partners.
- In addition, a cover article on plasmonic communications has been published in the May 2013 issue of Optics & Photonics News.
- A white paper on the innovation potential of plasmonic interconnects has been published online.
- Communication has been established with plasmonics-related EU-funded project PLATON (<http://www.ict-platon.eu>).
- The project website is up and running.
- A brochure on NAVOLCHI activities and goals has been issued.

- A press-release on the start of the project has been issued and another one has been submitted to the Photonics Unit newsletter.

In particular, the dissemination activities that have taken place are analyzed below per partner:

AIT is the leader of WP7. As such, AIT has already performed several activities related to the dissemination and promotion of the project results and technology. In the context of Milestone 45, AIT issued an official press release announcing the start of the project to the public. AIT designed and issued a brochure advertising NAVOLCHI. A white paper led by AIT and ST (where all partners contributed) on the innovation potential of plasmonic interconnects was prepared and posted online in the 1st year of the project. In the current period the following papers have been produced:

KIT

- “High Extinction Ratio and Energy Efficient Plasmonic Switch based on Reversible Nanofilament Formation”, Hoessbacher, C.; Fedoryshyn, Y.; Emboras, A.; Hillerkuss, D.; Melikyan, A.; Kohl, M.; Sommer, M.; Hafner, C.; Leuthold, J.; submitted to CLEO’2014
- 'High speed plasmonic phase modulators', Melikyan, A.; Alloatti, L.; Muslija, A.; Hillerkuss, D.; Schindler, P. C.; Li, J.; Palmer, R.; Korn, D.; Muehlbrandt, S.; Van Thourhout, D.; Chen, B.; Dinu, R.; Sommer, M.; Koos, C.; Kohl, M.; Freude, W.; Leuthold, J.; Nature Photonics, Advance online publication. doi:10.1038/nphoton.2014.9
<http://dx.doi.org/10.1038/nphoton.2014.9>
- 'Photonic to plasmonic mode converter', Melikyan, A.; Kohl, M.; Sommer, M.; Koos, C.; Freude, W.; Leuthold, J.; Optics Letters, to be submitted

TU/e

- V. Dolores-Calzadilla, A. Fiore, M. K. Smit, “Towards plasmonic lasers for optical interconnects”, IEEE Proceedings of the 14th International Conference on Optical Transparent Networks, 2012.
- V. Dolores-Calzadilla, D. Heiss, A. Fiore, M. K. Smit, “Metallo-dielectric nanolaser coupled to an InP-membrane waveguide”, Proceeding of the 17th Annual Symposium of the IEEE Photonics Society Benelux Chapter, 2012.
- D. Heiss, V. Dolores-Calzadilla, A. Fiore, M. Smit, “Design of a waveguide-coupled nanolaser for photonic integration”, Integrated Photonics Research, Silicon and Nano-Photonics, 2013.
- V. Dolores-Calzadilla, D. Heiss, A. Fiore, M. K. Smit, “Waveguide-coupled nanolasers in III-V membranes on silicon”, invited talk at IEEE Proceedings of the 15th International Conference on Optical Transparent Networks, 2013.

- V. Dolores-Calzadilla, D. Heiss, A. Fiore, M. K. Smit, “*Nanometallic lasers for optical interconnects*”, The 18th OptoElectronics and Communications Conference/Photonics in Switching, 2013.
- V. Dolores-Calzadilla, D. Heiss, A. Fiore, M. K. Smit, “*Fabrication technology of metal-cavity nanolasers in III-V membranes on silicon*”, Proceeding of the Proceedings of the 18th Annual Symposium of the IEEE Photonics Society Benelux Chapter, 2013.

Task 7.2 Exploitation

The main objective of this task is to explore the research outcomes of the NAVOLCHI project and promote market penetration of the end products. Due to the early stage of plasmonic technology, it is difficult to prepare for commercial products within or shortly after the timeframe of the project. At the same time, this early stage also means that project partners have the opportunity to lead the way in the technological advancement in their respective fields. In NAVOLCHI, this is mainly expressed through patent opportunities and innovative research through theses at the Master's and PhD level of participating institutions.

For a detailed list of exploitation activities, see D7.2. The main points are also summarized below.

- (UVEG) Patent: “Method to obtain metallic structures of nano- and micro-metric size from lithographic resists based on nanocomposites,, (P201201282).
 (“Método de obtención de estructuras metálicas de tamaño nano y micrométrico a partir de resinas litográficas basadas en nanocomposites)
- Theses (KIT, UGent, IMEC, UVEG):
 - (KIT) Calus Gaertner, “Plasmonic Modulators” (master thesis)
 - (UVEG) Henry Gordillo Millán, PhD thesis on Fabrication and characterization of polymer doped with quantum dots for photonic applications.
 - (UVEG) Mari Luz Martínez Marco, PhD thesis on conducting polymers containing metal nanoparticles and metal nano- and micro-structures using polymer-based patterns.
 - (UVEG) Víctor Latorre Garrido, “Propiedades Eléctricas y Ópticas del PMMA 3T-Au” (“Optical and electrical properties of PMMA-3T-Au”) (master thesis)
 - (UGent) Sukumar Rudra, “Diffractive Micro-Electromechanical Structures in Si and SiGe” (PhD Thesis).
 - (IMEC/UGent) Floris Taillieu, “Broadband colloidal quantum dot LED for active plasmonics” (master thesis).
 - (IMEC/UGent) Qi Lu, “Colloidal Nanocrystal Light Sources on Silicon”, (master thesis).
 - Other exploitation activities include the development of numerical tools of general interest (AIT), and several invitations to partners for papers and talks on NAVOLCHI technology (all).
- Exploitation plans at this point involve mainly attention to patent opportunities for the devices developed in the project, e.g.: TU/e-metallo dielectric laser, KIT-modulator,

UVEG/AIT-amplifier, IMEC-filers, etc. In addition, the consortium awaits the decisions on the new strategy at STMicroelectronics for further exploitation activities. See D7.2 for more information.

Task 7.3 Promotion

Task 7.3 has just been started and it is in progress.

Deliverables in reporting period month 1 – month 27

D7.1 First report on NAVOLCHI dissemination and promotion activities (m18) – submitted.

D7.2 First report on NAVOLCHI exploitation activities (m18) - submitted.

D7.3 Mirror Deliverable of D7.1, which will be available to the public on the website (m18) – submitted.

D7.4 Intermediate report on recent achievements (m18) – submitted.

Upcoming deliverables:

D7.5 Reports on the impact and outcome of organized promotion events (m36) –no delay expected.

D7.6 Final report on NAVOLCHI dissemination and promotion activities (m36) –no delay expected.

D7.7 Dissemination kit (m36) – no delay expected.

Milestones in reporting period month 18 - month 27

MS44 Dissemination of activities in the project's website and continuous update (m1) –met (ongoing ever since).

MS45 Press release on start of project distributed to the public (m2) –met.

MS46 Identification of possible contributions to the industrial partners for commercialization (m15) –delayed due to the reorganization process at ST.

Upcoming milestones

MS47 Organization of workshop on silicon photonics interface for chip-to-chip communication (m34) –no delay expected.

MS48 Public website for NAVOLCHI prepared to stay open for at least another year (m36) –no delay expected.

MS49 Press release distributed comprising key results with a public target audience (m36) – no delay expected.

3.3 Project Management (Work Package 1)

Beneath common management functions as

- Strategic management at project level,
- Control of work package activities, including technical quality control,
- Organisation of project reporting and meetings,
- Control of deliverable preparation,
- Conflict management,

the WP1 leader KIT is responsible for the quality management within the project during the complete projects run-time. The detailed list of management activities is given below.

Some administrative modifications became necessary after to the first reporting period (month 1-month 18) or are planned for the near future:

- Since June 2013, Prof. Dr. Jürg Leuthold (KIT / ETH) acts as Technical Project Manager and Prof. Dr. Manfred Kohl (KIT) is Coordinator (see 3.3.1).
- ST intends to reduce its engagement in work package 6 (see 3.3.6).
- The Consortium intends to extent the project activities by 6 month due to delays in development of fabrication technology and due to STs reduced engagement in WP6 (see 3.3.7).

3.3.1 Administrative Boards and Decisions

General Assembly:

The General Assembly as the prime board in this project is responsible for all major decisions within the project and consists of one representative of each party. It is chaired by the coordinator. No changes have been made compared to the previous reporting period. The members are listed below.

Karlsruhe Institute of Technology, Germany	KIT	Manfred Kohl
Interuniversity Microelectronics Centre VZW-IMEC, Belgium	IMEC	Dries Van Thourhout
Eindhoven University of Technology, Netherlands	TU/e	Meint Smit
Research and education laboratory in information technologies, Greece	AIT	Ioannis Tomkos
University of Valencia, Institute of Materials Science, Spain	UVEG	Juan Martinez Pastor
ST-Microelectronics, Italy	ST	Alberto Scandurra
Ghent University, Belgium	Ugent	Zeger Hens

Table 5: General Assembly.

Technical Project Manager and Project Management Committee:

In June 2013, Prof. Jürg Leuthold (KIT/ETH Zurich) and Prof. Manfred Kohl (KIT) switched their positions in the Project Management Committee. Prof. Jürg Leuthold became Technical Project Manager, Prof. Manfred Kohl became Coordinator. Reacting on STs diminished engagement in work package six, it will become necessary to replace ST by ETH as leader of that work package.

Technical Project Manager (Chair): Juerg Leuthold		
+		
Coordinator: Manfred Kohl		
+		
WP 1 Leader	KIT	Manfred Kohl
WP 2 Leader	AIT	Emmanouil-Panagiotis Fitrakis
WP 3 Leader	TU/e	Meint Smit
WP 4 Leader	UVEG	Juan Martinez Pastor
WP 5 Leader	IMEC	Dries Van Thourhout
WP 6 Leader	ST	Alberto Scandurra
WP 7 Leader	AIT	Dimitrios Klonidis

Table 6: Project Management Committee.

3.3.2 Management Deliverables

Deliverables covered by work package 1 with delivery dates are:

D1.1	Project web site with .eu domain (M01) and continuous update	11/2011
D1.2	Project reference online manual	01/2012
D1.3	Project quality assurance manual	04/2012
D1.4	Intermediate Progress Report 1	07/2012

All have been prepared in time, for access to the WEB-site and the manuals please follow the links.

3.3.3 Communication: Meetings and Phone Conferences

Up to now, seven meetings and 24 phone conferences have been held:

Meetings:

- 1) Kick-Off meeting in Karlsruhe, Germany, February 3rd 2012.
- 2) Intermediate Meeting in Warwick, Great Britain, July 6th 2012.
- 3) Meeting in Ghent, Belgium, November 26th 2012.
- 4) Project Review Meeting 1 in Brussels, Belgium, November 27th 2012.
- 5) Midterm Meeting in Karlsruhe, Germany, April 26th 2013.
- 6) Project Review Meeting 2 in Brussels, Belgium, July 10th 2013.
- 7) Meeting in Eindhoven, Belgium, January 28th 2014.

To provide a short reaction time on possible problems, it was decided that phone conferences will be held every month if applicable, typically on the first Monday of every month.

Phone Conferences:

1) November 16 th , 2011	9) November 5 th , 2012	17) June, 13 th , 2013
2) December 12 th , 2011	10) November 16 th , 2012	18) July 1 st , 2013
3) March 12 th , 2012	11) December 17 th , 2012	19) September 23 th , 2013
4) April 2 nd , 2012	12) January 14 th , 2013	20) October 14 th , 2013
5) May 7 th , 2012	13) February 4 th , 2013	21) November 4 th , 2013
6) June 4 th , 2012	14) March 4 th , 2013	22) December 4 th , 2013
7) September 3 rd , 2012	15) April 8 th , 2013	23) January 13 th , 2014
8) October 8 th , 2012	16) May 13 th , 2013	24) March 3 rd , 2014

Detailed documentation of partner presentations, results obtained and decisions made during the meetings and phone conferences can be found in the minutes-files available on our [WEB-site](#) (please follow the link).

3.3.4 Legal Status

No changes.

3.3.5 WEB-site

Since project start in November 2011, the WEB-site is available under www.navolchi.eu and is updated periodically. The WEB-Site is located at the Steinbuch Center for Computing (SCC), the IT- organization of the KIT, Karlsruhe. Due to a reorganisation of the server structure, detailed access information, broken down into country specific domains, can not be given anymore, contrary to the last report.

3.3.6 STs Reduced Commitment in Work Package 6

By beginning of 2014, ST informed the project partners that it will not be able to continue most of the remaining activities in WP6. As ST is the actual leader of WP6, a reorganisation of the tasks and responsibilities will be necessary. Despite these obstacles, the consortium is confident to redistribute and fulfil the remaining tasks. As a major action, the NAVOLCHI consortium decided that ETH should become a new partner of the NAVOLCHI consortium and take over the full responsibility for all duties of ST in WP6. For the remaining work in tasks 6.3 and 6.4, ST will take over the role of a consultant. **For all other tasks in WP6 as well as in all other WPs, ST will keep its active role as before.**

The current scenario is as follows:

- Actual situation: WP6 consists of four tasks, while in task 6.1 no contribution of ST has been planned and in task 6.2 ST has support activities only. **So both tasks 6.1 and 6.2 require no reorganisation of ST activities.**
- Resources: The originally planned ST contribution in tasks 6.3 and 6.4 amounts to 19.5 man months (MM, equivalent to € 85.800) and € 46.200 for consumables, which have to be redistributed.
- Course of action: ETH will take over all duties of ST in tasks 6.3 and 6.4. KIT will support ETH and closely collaborate to fulfil this task. In particular, KIT will provide the required input for layout and characterization of the plasmonic transmitter in the demonstrator system. ST will contribute with a total effort of two MM as a consultant. This will guarantee a continuity of the work and an effective transfer of the results obtained so far. The corresponding redistribution of the resources is listed below:

To be redistributed	New share of ST	New share of ETH
19.5 MM	2 MM	17.5 MM
Personnel: € 85.500	€ 8.800	€ 77.000
Consumables: € 46.200	-----	€ 46.200

Table 7: Redistribution of resources in WP6.

ETH is capable to meet all the requirements that are needed to continue STs work and to fulfil the outstanding tasks of WP6. This covers:

- Carrying out an analysis of the developed chip to chip interconnect for transmitter side and receiver side.
- Assembly of all building blocks and generating a complete system.

- ETH becomes work package leader of WP6

Once the reorganization of the financial resources is approved by the EC, ST will reimburse the agreed amount of money to the coordinator, who remits the money to ETH.

Financial consequences

A reorganization of the financial resources will be necessary to continue WP6 after the retreat of ST. With the last payment from the EC, ST obtained more funding as compatible with the new plans of STs engagement in the project. Therefore, ST has to reimburse a certain amount. To calculate the reimbursement correctly, not only the second tranche already paid but also the final tranche has to be taken in to account. The detailed calculation follows below:

Originally planned according to GA before STs retreat:

- Previous payment done to ST (tranche 2, T2): 102.3 t€
- Final payment to ST scheduled after successful end of the project (final tranche, TF): 69.4 t€
- Total payment to ST after month 18 scheduled (T2+TF): 102,3 t€ + 69.4 t€ = **171.7 t€**

Calculation of STs reimbursement after STs retreat:

- Total MM of ST to be redistributed: 19.5 MM (corresponding to 4.4 t€/MM)
- Total consumables of ST to be redistributed: 46.2 t€
- Total amount to be redistributed: 85.8 t€ + 46.2 t€ = 132 t€

We highly appreciate that ST plans to act as consultant in WP6, which is taken into account by 2 MM in WP6.

- Therefore, the total amount to be redistributed reduces to: 132 t€ - 8.8 t€ = **123.2 t€**

STs share remaining after STs retreat:

- Total payment to ST after month 18 to be scheduled: 171.7 t€ - 123.2 t€ = **48.5 t€**
- The corresponding payments T2 and TF to be scheduled are: 48.5 t€ = 28.9 t€ (T2) + 19.6 t€ (TF)

STs reimbursement, broken down to tranches T2 and TF:

- The amount of tranche 2 (T2) that ST should reimburse is: 102.3 t€ - 28.9 t€ = **73.4 t€**
- The amount of the final tranche (TF) to be redistributed to other partners is: 69.4 t€ - 19.6 t€ = **49.8 t€**

ST has been asked by the coordinator about a confirmative acceptance of the reimbursement calculated above and to initiate it. A provisional acceptance was given to the coordinator.

3.3.7 Project Extension, Agreements and Confirmations

By decision of the management board at the NAVOLCHI Meeting in Eindhoven, January 28th 2014, **project partners agreed to apply for an extension of the project by 6 months**. Main reasons for this action are the retreat of ST from WP6 as well as a number of technical reasons, particularly

- Complexity of modulator fabrication with sufficient performance (KIT),
- Availability of QDOTs with satisfactory gain (IMEC, UGent, UVEG),
- Difficulties in fabrication of nanolaser (TUE),

which cause the need to reschedule the related deliverables and milestones. Additionally, a successful system integration and a significant estimation of techno-economic impact of the complete system (AIT) depend on the topics listed above.

The following section contains a more detailed summary of explanations from each partner why they propose an extension of the project. In addition, all partners confirm that they agree to extend the project by six months.

Confirmation of KIT agreement to extend the project by 6 months

Results obtained from the first / second generation of modulators revealed issues in the fabrication part of the work that need to be solved before the plasmonic modulators can be used in the real chip-to-chip interconnect systems. Particularly, the following improvements should be made to enhance the modulators performances:

Plasmonic phase modulator:

- 1) Optical loss reduction by reducing the metallic slot size and by shortening the device
- 2) Improvement of the signal quality by using better electro-optic polymers

Plasmonic absorption modulator:

- 1) Increasing the speed of the modulator
- 2) Improving the fabrication process

Taking into account the real challenges involved in the above tasks, we think an extension of the project will be needed for reaching the project goals.

Confirmation of IMEC agreement to extend the project by 6 months

IMEC's tasks in the project are related to:

WP5 (design of filters, design of couplers)

WP4 (design and fabrication of plasmonic amplifier)

Providing Ge-detector chips as back-up solution for building link

While tasks related to WP5 and Ge-detector are progressing well, for WP4 (optical amplifier) IMEC is relying on the availability of QDOTs exhibiting gain. As explained by UGent the availability of these QDOTs have been delayed but there is good hope such QDOTS will become

available soon. Hence our work would strongly benefit from a project extension since it will allow us to make use of the new generation amplifiers to realize the requested optical amplifier.

Confirmation of TU/e agreement to extend the project by 6 months

The nanolaser device has been identified as a key component for one of the scenarios considered for the final project demonstrator, in which the nanolaser is directly modulated. Although its fabrication is promising, at the moment we are lying behind the time schedule because we have not achieved lasing yet. In view of the current fabrication progress, a project extension by six months will enable us to carry out further technology development to solve the issues encountered during the first fabrication run. In this way, further runs will be promising to demonstrate lasing and make the directly modulated nanolaser a realistic scenario for the final demonstrator.

Confirmation of AIT agreement to extend the project by 6 months

AIT supports and agrees on the extension of the NAVOLHCI project for 6 months. The additional time is essential as it will enable us to perform the techno-economic evaluation and the study of the system based on the latest characteristics of the new devices that will be developed by the other partners. Furthermore, the additional time is required to face the transition of some tasks from ST to other partners. We believe that the additional time will give us the chance to further strengthen the project and to enhance the quality of the developed NAVOLCHI system.

Confirmation of UVEG agreement to extend the project by 6 months

UVEG's tasks in the project are related to:

WP4:

- (1) Design, fabrication and characterization of plasmonic amplifier using quantum dots (QDs) dispersed in a polymer,
- (2) Design, fabrication and characterization of plasmonic photodetectors based on QDs (Schottky photodiode, micro- and nano-gap photoconductors)

A lot of work has been carried out within WP4 during these two years and progress made from the point of view of materials for photodetectors and concepts/designs for using in plasmonic amplifiers. At the moment, plasmonic amplifiers depend on the availability of QDs exhibiting net gain. As explained by UGent the availability of these QDs has been delayed but there is good hope such QDs will become available soon. Hence our work would strongly benefit from a project extension since it will allow us to fabricate our plasmonic amplifier concepts using this promising material. Whereas Schottky photodiodes based on PbS quantum dots are now giving good responsivity at 1.5 μm we would also benefit of the project extension to fabricate and test nano-gap waveguide photoconductors (other than micro-gap versions) based on the same absorbing material.

Confirmation of ST agreement to extend the project by 6 months

ST faced different reorganizations during the last 2 years, the last one having a deep impact on the project; in fact the ST group responsible for on-chip and off-chip communication (ISG, Interconnect Systems Group) has been closed, and all its resources have been moved to microcontroller division (MCD), having no business interest in chip to chip interconnect.

For this reason a certain delay has been accumulated in some activities, and because of the closure of ISG ST can no longer carry out the activities foreseen by WP6.

The requested 6 months extension would allow ST to complete accurately all the scheduled activities and the consortium to take the proper actions to carry out all the activities foreseen by WP6.

Confirmation of UGent agreement to extend the project by 6 months

In view of our work on a quantum dot based gain medium for optical amplification on chip, this extension will enable us to transfer the results we have obtained so far on HgTe QDs in solution to HgTe QDs in a thin film and test these films for optical amplification after deposition on SOI waveguides. As mentioned for the first time during the review meetings of July 2013 and confirmed in all follow up meetings, we observe long-lived, low-threshold gain in dispersions of HgTe QDs with gain coefficients that are sufficient to make optical amplification on chip feasible. Unfortunately, first attempts to translate these results to HgTe QDs in thin films have failed. According to our current understanding, this is due to the gain being related to an electronic transition between the conduction band and an empty surface trap, which appears to get occupied during the currently used film formation method. Extending the project with 6 months will enable us to (1) explore improved methods to make films of HgTe QDs – where we first plan to embed them in polymers – (2) analyse the gain characteristics of these films using transient absorption spectroscopy and (3) deposit the HgTe QD / polymer composite on SOI or plasmonic waveguides and test optical amplification by these structures.

3.3.8 Management Summary

As stated in the reports concerning the work packages 2-5 and 7, all deliverables and milestones of the first report period have been accomplished successfully. Deliverables 6.1 and 6.2 will be delayed due to a number of technical reasons. In order to consider the reduced activity of ST in WP6 and to cope with the accumulated delays, the tasks in WP6 need to be reorganized including ETH as a new partner, and it will be important to extend the project by six months. We are confident that these steps are appropriate to meet the remaining challenges of the project.

3.4 Deliverables and Milestones Tables

3.4.1 Deliverables

Status levels: finished in progress due critical





Deliverable		WP	Partner	Type	Diss	Delivery	
Nr.	Title					Mnth	Date
 D1.1	Project web site with .eu domain (M01) and continuous update	1	KIT	O	PU	1	11/2011
 D1.2	Project reference online manual	1	KIT	O	RE	3	01/2012
 D2.1	Definition of chip-to-chip interconnection system environment and specification	2	ST	R	RE	3	01/2012
 D1.3	Project quality assurance manual	1	KIT	O	RE	6	04/2012
 D5.1	DDCM specification document	5	ST	R	CO	6	04/2012
 D1.4	Intermediate progress report (1)	1	KIT	R	PU	9	07/2012
 D2.2	Definition of plasmonic devices	2	AIT	R	RE	12	10/2012
 D3.1	Report on studies of optimized structure for metallic / plasmonic nano-laser and its coupling to Si WG	3	TU/e	R	CO	12	10/2012
 D3.2	Report on modelling of the modulator structure	3	KIT	R	CO	12	10/2012
 D5.2	DDCM with electrical PHY design and verification data base	5	ST	R	CO	12	10/2012
 D4.1	Designs of plasmonic amplifiers	4	AIT	R	CO	18	04/2013
 D4.2	Report on optical properties of QDs layers and polymer nanocomposites	4	AIT	R	PU	18	04/2013
 D7.1	First report on NAVOLCHI dissemination and promotion activities	7	ST	R	RE	18	04/2013
 D7.2	First report on NAVOLCHI exploitation activities	7	AIT	R	RE	18	04/2013
 D7.3	Mirror Deliverable of D7.1, which will be available to the public on the website.	7	TU/e	R	PU	18	04/2013
 D7.4	Intermediate report on recent achievements.	7	AIT	R	PU	18	04/2013
 D5.3	Compact optical filters (2nm bandwidth, >30nm FSR) and first generation beam shapers	5	IMEC	R	CO	21	07/2013
 D2.3	Investigation of chip-to-chip interconnection level specifications employing new plasmonic devices	2	AIT	R	RE	24	10/2013
 D2.4	Interface and plasmonic interconnect models and reports	2	ST	R	RE	24	10/2013

Table 8: Deliverables of the NAVOLCHI project, ordered by delivery date.

D3.3	Fabrication of plasmonic laser device	3	TU/e	R	CO	24	10/2013
D3.4	Report on fabrication of modulators	3	KIT	R	CO	24	10/2013
D4.3	Designs of plasmonic photodetectors	4	AIT	R	CO	24	10/2013
D5.4	Generic DDCM compatible with plasmonic-based PHY specification document	5	ST	R	PU	24	10/2013
D5.5	Report on plasmonic waveguide couplers	5	KIT	R	CO	24	10/2013
D1.5	Intermediate progress report (2)	1	KIT	R	RE	27	01/2014
D6.1	Report on characterization results of all plasmonic devices	6	TU/e	R	RE	27	01/2014
D6.2	Report on characterization results of all optical interface plasmonic passive components	6	KIT	R	RE	27	01/2014
D2.5	Technoeconomical evaluation with respect to the cost efficiency and green aspects	2	AIT	R	PU	30	04/2014
D4.4	Report on SPP amplifiers by using QDs	4	IMEC	R	PU	30	04/2014
D5.6	Generic DDCM compatible with plasmonic-based PHY design and verification data base	5	ST	R	CO	30	04/2014
D4.5	Report on plasmonic photodetectors	4	UVEG	R	PU	33	07/2014
D5.7	Second generation beam shapers (distance 1mm, with bandwidth > 10nm and efficiency > 3dB)	5	IMEC	P	CO	33	07/2014
D2.6	Report on new applications and their opportunities	2	AIT	R	PU	36	10/2014
D6.3	Report on chip to chip interconnect characterization	6	ST	R	PU	36	10/2014
D6.4	Report on plasmonic chip-to-chip interconnect prototype testing and evaluation	6	AIT	R	PU	36	10/2014
D7.5	Reports on the impact and outcome of the organized promotion events.	7	AIT	R	PU	36	10/2014
D7.6	Final report on NAVOLCHI dissemination and promotion activities	7	AIT	R	RE	36	10/2014
D7.7	Dissemination kit	7	AIT	O	PU	36	10/2014

Table 9: Deliverables of the NAVOLCHI project, ordered by delivery date (continued).

Diss: PU = Public

PP = Restricted to other programme participants (including the Commission Services).

RE = Restricted to a group specified by the consortium (including the Commission Services).

CO = Confidential, only for members of the consortium (including the Commission Services).

3.4.2 Milestones

Status levels: finished in progress due critical



















Milestone		WP	Partner	Delivery	
Nr.	Title			Mnth	Date
 MS44	Dissemination of activities in the project's web site and continuous update	7	KIT	1	11/2011
 MS45	Press release on start of project to the public distributed	7	AIT	2	12/2011
 MS1	Definition of chip-to-chip interconnection system environment and specification	2	AIT	3	01/2012
 MS2	Definition of plasmonic devices and material properties for chip-to-chip interconnection	2	AIT	6	04/2012
 MS8	Decision on an optimized structure for metallic/plasmonic nano-laser and its coupling to Si waveguide	3	TU/e	6	04/2012
 MS9	Decision on an optimized structure for plasmonic modulator	3	KIT	6	04/2012
 MS25	Decision on optimized plasmonic waveguide couplers	5	KIT	6	04/2012
 MS10	Grown wafer structure for plasmonic lasers	3	IMEC	12	10/2012
 MS16	Decision on optimized structures for plasmonic amplifiers	4	UVEG	12	10/2012
 MS17	Synthesis of nanoparticles with gain at 1550nm	4	Ugent	12	10/2012
 MS26	Fabrication of plasmonic waveguide couplers with less than 3 dB coupling loss	5	KIT	12	10/2012
 MS27	Design of first generation beam shapers and compact optical filters	5	IMEC	12	10/2012
 MS28	DDCM with electrical PHY design and verification	5	ST	12	10/2012
 MS37	Plasmonic active device characterization results	6	KIT	12	10/2012
 MS11	Fabrication of plasmonic modulator on a SOI platform	3	KIT	15	01/2013
 MS18	Demonstration of conductive QD layers with photoconductive properties	4	UVEG	15	01/2013
 MS19	Demonstration of metal-(lithographic) polymer and QD metal-(lithographic) polymer nanocompo-sites	4	UVEG	15	01/2013
 MS29	Data codecs for power consumption reduction	5	ST	15	01/2013

Table 10: Milestones of the NAVOLCHI project, ordered by delivery date.


















 MS30	Decision on plasmonic waveguide couplers with less than 3 dB coupling loss	5	KIT	15	01/2013
 MS46	Identification of possible contributions to the industrial partners for commercialization	7	ST	15	01/2013
 MS3	Development of a system and device simulation platform	2	AIT	18	04/2013
 MS4	Definition of the interconnection level specification employing developed plasmonic photonic devices	2	ST	18	04/2013
 MS12	Decision on an optimized structure for plasmonic modulator with a maximum loss of 20dB	3	KIT	18	04/2013
MS13*	Initial characterization of unbonded plasmonic lasers	3	TU/e	18	04/2013
 MS20	Demonstration and decision on photodetector operation: nano-gap (MIM) vs. Schottky / heterostructure	4	UVEG	18	04/2013
 MS21	Electroluminescence from QD stack embedded within conductive oxides ($>1\mu\text{W}$)	4	IMEC	18	04/2013
 MS31	Fabrication of compact optical filters and first generation beam shapers	5	IMEC	18	04/2013
 MS32	Data codecs for error detection and correction	5	ST	18	04/2013
 MS5	Digital domain to plasmonic domain interface specification and VHDL modelling	2	ST	21	07/2013
 MS14	Initial testing and characterization of plasmonic modulators	3	KIT	21	07/2013
 MS22	Demonstration of plasmonic amplifiers with optical pumping exhibiting 10dB gain  Appendix A	4	IMEC	21	07/2013
 MS6	Plasmonic interconnect VHDL modeling	2	ST	24	10/2013
 MS15	Initial testing of bonded plasmonic lasers	3	TU/e	24	10/2013
 MS23	Operation of QD based photodetector with responsivity $> 0.1\text{A/W}$	4	UVEG	24	10/2013
MS33	Design of second generation beam shapers	5	IMEC	24	10/2013
 MS34	Generic DDCM compatible with plasmonic-based PHY	5	ST	24	10/2013

Table 11: Milestones of the NAVOLCHI project, ordered by delivery date (continued).

MS38	Plasmonic passive components characterization results with a 1dB coupling loss	6	KIT	24	10/2013
MS39	Concept for system integration developed	6	AIT	27	01/2014
MS7	Investigation of the cost and power consumption efficiency of the developed plasmonic devices	2	AIT	28	02/2014
MS24	Demonstration of SPP amplifiers with electrical injection exhibiting 10dB/cm gain	4	UVEG	30	04/2014
MS35	Fabrication of compact optical filters and first generation beam shapers	5	IMEC	30	04/2014
MS36	DDCM evolution for NiP solutions	5	ST	30	04/2014
MS40	Individual plasmonic devices characterization, testing and evaluation	6	TU/e	30	04/2014
MS41	Chip to chip interconnect characterization	6	ST	33	07/2014
MS42	Plasmonic components integration to demonstrate chip-to-chip interconnect	6	AIT	33	07/2014
MS47	Organization of workshop on silicon photonics interface for chip-to-chip communication	7	TU/e	34	08/2014
MS43	Plasmonic chip to chip interconnect prototype testing and evaluation	6	ST	36	10/2014
MS48	Public web site for NAVOLCHI prepared to stay open for at least another year	7	KIT	36	10/2014
MS49	Press release distributed comprising key results with a public target audience	7	AIT	36	10/2014

*: MS13 has been identified as inappropriate to the course of the project and was skipped in agreement with EC

Table 12: Milestones of the NAVOLCHI project, ordered by delivery date (continued).

Comment to MS8: A suitable structure based on a plasmonic laser was designed, however further investigations are being carried out to design a metallic laser, which might offer a better performance.

4 Attachments

As determined in the projects “Description of Work”, the milestones (refer to chapter 3.4.2) achieved so far are delivered with this report. To avoid redundant lengthening of this document, the milestones are delivered as separate files. Additionally, you can find them on our web site www.navolchi.eu.