Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Definition of Plasmonic Devices

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Executive Summary

This document presents the main targeted characteristics for the devices that will constitute the interconnect system we aim to develop. Recent changes of implementation methods are included, where applicable. Benchmarking data and system goals initiate the document in order to present the context.

Change Records

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1. Introduction

Today, electronics is limited in operating speed, while photonics is limited in miniaturization capability. By use of the emerging science of plasmonics, NAVOLCHI aims to bridge the gap between electronics and photonics, thus paving the way for the faster and smaller chip technology of the future.

In NAVOLCHI, the interconnect will comprise plasmonic transceivers: Key elements to be developed are plasmonic lasers and modulators for the transmitter, plasmonic amplifiers and detectors for the receiver. The plasmonic devices will be monolithically integrated on an industry-friendly CMOS platform.

In particular, the plasmonic interconnect system will consist of the following devices:

Table I:

Type	**Device**	**Leader**
Transmitter	Plasmonic Nano-Laser	TU/e
Trasnmitter	Plasmonic Modulator	KIT
Receiver	Plasmonic Amplifier	UVEG
Receiver	Plasmonic Photodetector	UVEG
Supporting Components	Waveguide Coupler	KIT
Supporting Components	Noise Filter	IMEC
Supporting Components	Beam Steering	IMEC
Supporting Components	Signal Generation Module	ST

The following sections present the targeted specifications for each of the above devices. But first, we will review the system goals and some initial benchmarking in order to have a view of the context.

2. Benchmarking

In NAVOLCHI, proper benchmarking will take place in Task 2.4 in the 3rd year of the project. Nevertheless, initial benchmarking has already been conducted in order to guide the setting of the project goals.

In 2010, the state-of-the-art optical transceivers consumed tens of pJ/bit [1].

Benchmarking data follows:

Table II: Benchmarking

Link	Type	Throughput	Latency	Power	Pins
Intel 50G Link [2]	Opt.	50 Gb/s (12.5x4)			
UNIC [1]	Opt.	5 Gb/s*		5 mW*	
TI C2C [3]	Electr.	6.4 Gb/s	50 ns		16
MIPI LLI [4]	Electr.	5.8 Gb/s	80 ns	15pJ/bit	4
MIPI UniPort [4]	Electr.	3.2 Gb/s (0.8x4)	high	15pJ/bit	4

*first-year results of research project.

Intel's 50G Silicon Photonics Optical Link uses lasers to transmit data between two silicon chips, a transmitter and a receiver. It is composed of four optical channels, each running at 12.5 Gb/s, which are combined onto a single fiber to transmit data up to 50 Gb/s.

The Ultra-performance Nanophotonic Intrachip Communication (UNIC) is a DARPA-funded project that involves Sun/Oracle, Kotura and Luxtera. It started in 2008 and finishes in 2013. UNIC aims to achieve "unprecedented high-density, low-power, large-bandwidth, and low-latency optical interconnect for highly compact supercomputer systems". UNIC first-year achievements included a 320 fJ/bit hybrid-bonded optical transmitter and a 690 fJ/bit hybrid-bonded optical receiver. The project utilizes silicon photonics and assumes an external laser. In 2010, the power consumption target for

2012 was 300 fJ/bit, two orders of magnitude lower than state-of-the-art optical transceivers.

TI C2C (available since 2010) contains technology from Texas Instruments and Arteris. It was created to allow DRAM memory sharing for reduced eBoM cost through a very low latency interface. C2C does not require a PHY. C2C requires about 30 pins total in a mobile phone use model (16 transmit pins, 8 receive pins, plus clock and power pins). Round trip latency is 100 ns. It requires 1.2 or 1.8 volts and has throughput of 6.4 Gb/sec at 200 MHz DDR speeds and using 16 pins.

The UniPro specification was first released in 2007. UniPort is UniPro combined with a MIPI D-PHY or M-PHY. It supports a maximum data rate of 800 Mbit/s per lane, for 1 to 4 lanes. UniPro is not low latency enough for RAM sharing.

The MIPI LLI specification was released in 2011, but we only have targeted specs. Its primary purpose was to allow sufficient performance to enable sharing a DRAM memory. The main motivation was electronic bill of materials (eBoM) cost reduction. Round trip latency was targeted to be 80 ns using 8 pins in Gear 3. Unidirectional throughput is 2.9 Gb/s per lane using Gear 2.

3. System Goals

The goal of this project is to realize chip-to-chip and system-in-package chip-to-components plasmonic interconnects with the smallest footprint, power consumption, and latency at high bit-rates by introducing novel plasmonic, CMOS compatible photonic technologies.

In the 6th month of the project, specific system goals were set. The targeted specs were based on input by industrial partner ST Microelectronics, as well as on the intial benchmarking that was presented in Section 2.

Table III: Plasmonic interconnect targeted specifications

Data Rate	7.2 Gb/s
Latency	< 8.88 ns @450 MHz clock*
Power Consumption	<15 pJ/bit
Size	The target for each device will be to beat the diffraction limit.

*In case of faster electronics, latency will have to be lower.

As NAVOLCHI is a very ambitious research project that utilizes cutting-edge science, some targets may not be fulfilled in its duration. It will be in Task 2.2 where system simulations will take place and set goals may have to be adjusted.

4. Transmitter

The plasmonic interconnect will comprise a metallo-dielectric laser and a plasmonic modulator.

a) Metallo-dielectric Laser

It is the aim of WP3 to develop a laser with a metallic cavity coupled to a silicon waveguide. We have previously reported the design of a plasmonic laser with a low performance in Milestone 8. Here, the design for a metallo-dielectric nanolaser with electrical injection and coupled to an InP-membrane waveguide is presented. The structure supports a dielectric lasing mode near 1.55 μm with a high Q-factor due to a reflective metallic cladding. Threshold gain levels below 1000 cm^{-1} are predicted, which are compatible with room temperature operation under a current injection of a few tens of microamperes. Due to an efficient coupling to the waveguide and an expected low threshold current operation, it has been decided to carry out the fabrication of the metallo-dielectric laser described in this report. A metallo-dielectric cavity laser coupled to a waveguide on a III-V membrane bonded with BCB to silicon is thus described.

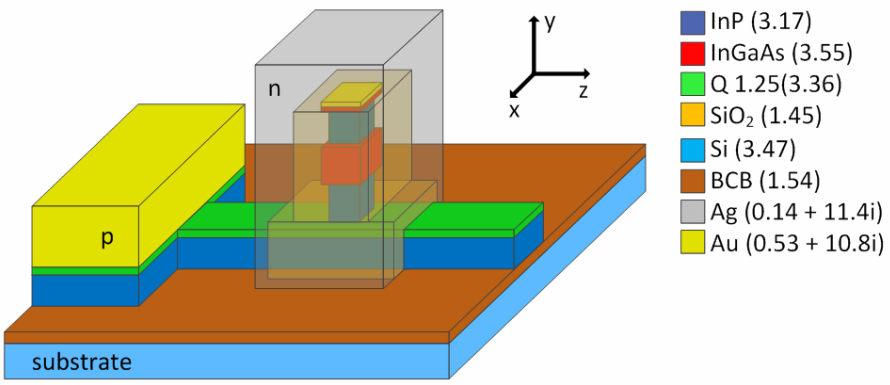

Figure 1. Model of the metallo-dielectric laser coupled to an InP-membrane waveguide. The refractive index of each material at 1.55 μm is shown in parenthesis.

The proposed laser structure is shown in Fig. 1. The semiconductor laser pillar lies on top of a thin InP waveguide and it is insulated with a SiO_2 layer from a metallic cladding. A lateral p-contact is electrically connected to the pillar through a highly doped quaternary (InGaAsP) layer. The metallic cladding acts itself as the n-contact allowing a top-down current flow. For simplicity, Fig. 1 does not show the ohmic contact layers Ti/Pt/Au, however they were included in the simulation model in order to consider their optical loss.

The optimized cavity has an insulation thickness of 175 nm to maximize the Q-factor, a bottom post height of 400 nm and a cavity length of 400 nm to provide a high differential efficiency. This results in a low threshold gain of 815 cm^{-1}, which can be reached with a current injection of about 70 μA at room temperature. Due to the better performance of the metallo-dielectric nanolaser compared to the plasmonic laser previously reported [5], we have decided to carry out its fabrication.

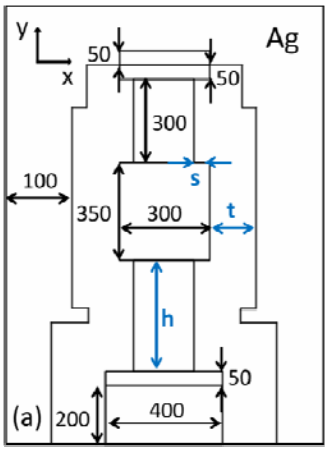

Figure 2: Schematic of the cavity with dimensions in nanometers. The optimization parameters are shown in blue.

The following table summarizes the expected parameters of both, the previously reported plasmonic laser and the metallo-dielectric laser described in this document.

Table IV: Laser characteristics

Parameter	**Plasmonic laser (at cryogenic temperatures)**	**Metallo-dielectric nanolaser (at room temperature)**
Wavelength	$1.4 - 1.55\ \mu m$	$1.55 \pm 0.1\ \mu m$
Driving voltage	$< 3\ V$	$< 6\ V$
Current	$< 3\ mA$	$< 1\ mA$
Device length	$> 10\ \mu m$	$< 1\ \mu m$
Output power	$> 10\ \mu W$	$> 50\ \mu W$

Remarks:

- The operating wavelength in the plasmonic laser is limited by the high current injection needed to produce enough gain to overcome the large modal loss, whereas in the case of the metallic laser is mainly limited by the fabrication accuracy.

- The operating current in the metallic laser is expected to be lower due to a reduced metal loss and also because the device is smaller.
- Only long (several tens of micrometers) plasmonic lasers are suitable for room temperature operation. The metallic laser is expected to have a sub-micron length.
- The maximum output power is limited by the self-heating of the devices. Accurate thermal simulations would be required in order to predict it accurately.
- We have decided to fabricate the metallic laser due to its better performance. The table shows the expected values of our current design, however we are working on further improvements in order to reach $100\ \mu W$ of output power, as well as to reduce the operating voltage.

Deliverable 3.1 contains more information on the laser.

b) Plasmonic Modulator

As a result of overall modelling the following modulator characteristics are obtained, see NAVOLCHI Deliverable 3.2:

Table V: Plasmonic modulator characteristics

Operation wavelength	1.55μm	☺	Insertion loss	< 20dB	😐
Total length	< 50μm	☺	Data Rate	>50Gb/s	☺
Maximum voltage	$4.5V_{pp}$	☺	Latency	<3 ps	☺
Silicon compatibility	yes	☺	Electrical energy consumption	15 pJ/bit	😐

Most of the required specification on the modulator can be fulfilled employing a plasmonic phase modulator. It is relatively more challenging to reduce the optical losses in the system.

We are currently carrying out fabrication and characterization of the plasmonic couplers and modulators fabricated on SOI chips provided by IMEC. In figure 3, we show an SEM image of the complete plasmonic phase modulator comprising two taper couplers and metallic nanoslot in between.

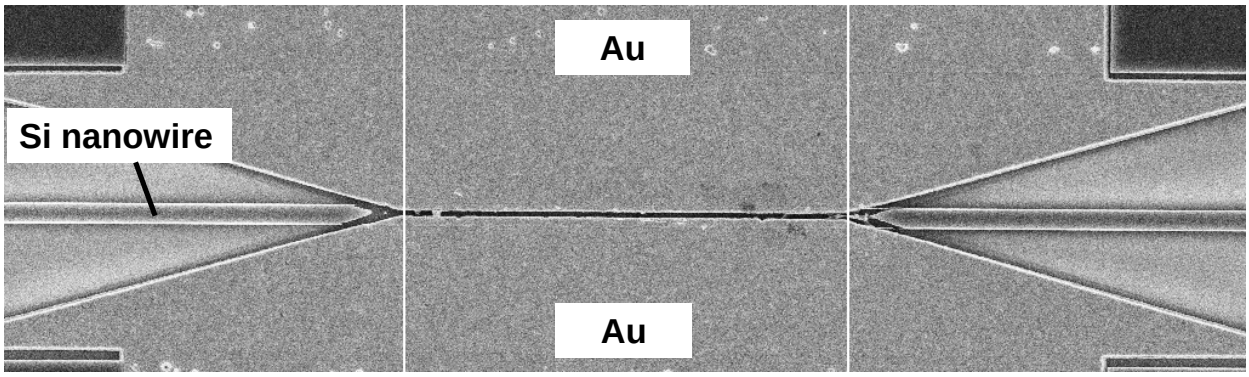

Figure 3 Scanning electron microscope image of the plasmonic phase modulator.

5. Receiver

The receiver will consist of the plasmonic pre-amplifier and the plasmonic photodetector.

a) Plasmonic Amplifier

Since the transmitter is expected to deliver a low signal level, the first element in the receiver is a plasmonic amplifier able to provide a 10 dB gain at the operation wavelength. This operation is necessary to supply the appropriate power to be measured by the photodetector with a good signal to noise ratio. Such amplifier has the requirements to be integrated in a silicon platform and operate under either optical or electrical pumping. For this purpose technologies based on active polymer and colloidal quantum dots nanocomposites and SOI waveguides are being studied.

IMEC and UVEG are developing a pre-amplifier for the receiver to be incorporated in the NAVOLCHI optical link. The amplifier will use a novel material, colloidal quantum dots, as the gain medium. The first aim is to demonstrate actual gain in these devices. The second target is to demonstrate optical injection. Regarding the system targets, the following can be said:

-Data rate: The device is operated in DC, under constant power. Therefore foreseen data rate is expected to pose no challenge.
-Latency: the amplifier will not introduce latency beyond the time needed to traverse the device (c/(nL) with L 100-500 μm)
-Power consumption: power consumption is the main issue for an amplifier. Assuming 100mW DC power consumption, leads to approx. 10pJ/bit (at 10GBit/s), almost consuming the full power budget for the link. Amplifying several wavelength signals simultaneously however might decrease the per pit power consumption.
- SNR: the amplifier by definition will add noise to the system. The precise level will depend on the efficiency of the amplifier and loss sources and remains to be determined.
- Device size: w = 5 μm, L=100-500 μm
- Loss: positive gain is expected
- Input requirements: NA

Table VI: Plasmonic amplifier characteristics

Data Rate	DC operation
Length	< 500 μm
Width	5 μm
Power Consumption	~10 pJ/bit*
Gain	10 dB
Latency	**

* Work in progress. See text.
** See text.

Refer to milestone 16 for more information on the plasmonic amplifier.

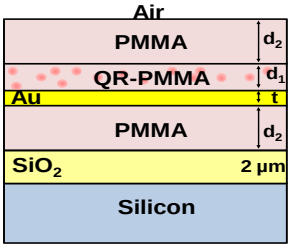

Figure 4: One of the plasmonic amplifier designs that will be tried. A 30 nm-thick gold film is sandwiched between PMMA layers that are doped with colloidal quantum dots. Refer to Milestone 16 for more information.

b) Plasmonic Photodetector

Reported responsivities in recent literature are in the range of 0.1-3.9 A/W for a PbS QD monolayer in a nanogap photoconductor, larger than 100 A/W for a PbS layer thicker than 200 nm in an inter-digitated electrode 10 µm x 3 mm, and more than 10^6 A/W in a MOS structure based on a PbS layer (60-80 nm thick) on graphene.
Another possibility is the direct conversion of plasmons (produced by incoming light at metal nanostructures into electrons if they are embedded in conductive polymer (recently demonstrated for metal nanoparticles in TiO_2).

Table VII: Parameters for plasmonic photodetector.

Parameter	**Targeted Value**
Quantum Efficiencies	> 80%
Responsivities	> 0.1 A/W

Regarding response time of above proposed photoconductive devices will depend on the transit time that can be reached for a given gate voltage. The best mobility values reached by QD-solids are in the range of 0.1 – 1 cm^2/Vs and much lower in conducting polymers (or long-ligand QD-solids). For a gate distance of 10 µm, 1-10 µs per V would be thus a minimum value for transit time. In principle, for 10 V, highest mobility, and 5-10 micron gate, a delay of 50-100 ns could be reached. This latency is high in comparison to the system goals and further research is required in order to find ways to reduce this number.

6. Supporting components

The supporting components include the waveguide couplers, beam steering, the noise filters and the signal generation module.

a) Waveguide coupler

Referring to the decision made on plasmonic modulator design (see D3.2), efficient couplers are necessary which will provide good coupling between the low loss silicon nanowire waveguide and the plasmonic vertical slot waveguide. The most promising approach to couple light from a silicon nanowire to a plasmonic slot waveguide is the tapered metallic coupling configuration which provides very large and broadband coupling efficiency. In such a coupling scheme, quasi-TE polarized light guided through silicon nanowire is adiabatically squeezed and launched into the plasmonic slot waveguide, see Fig. 5.

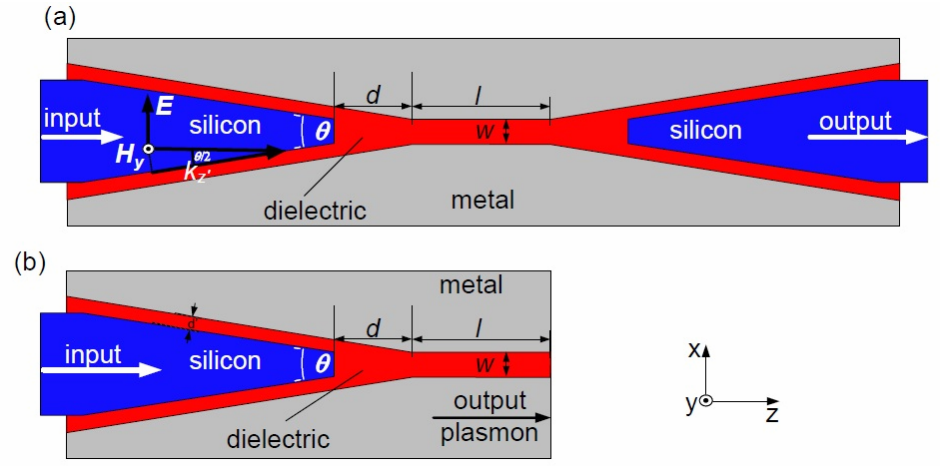

Figure 5: Geometry of plasmonic coupler, (a) top view of the realistic plasmonic modulator with two coupling sections and (b) structure used in optimization

Parameters for the coupler can be found in the following table.

Table VIII: Parameters for waveguide coupler.

Parameter	**Value**
SOI device layer thickness	220 nm
Silicon waveguide width	500 nm
Plasmonic slot width	50 nm
Distance *d*	75 nm
Angle *θ*	36°
Efficiency of a single coupler	87%

b) Noise Filter

Table IX: Parameters for noise filter.

Parameter	**Targeted Value**
Bandwidth	3 nm
Suppression	10 dB
Free Spectral Range	30 nm

Implementation: AWG with flat-top passband (MMI-input based).

c) Dual Die Communication Module (DDCM)

The DDCM, Dual Die Communication Module, is a hardware building-block allowing the communication between different dice within the same package, enabling the so-called System in Package (SiP) technology.
It is available as a soft IP, i.e. a synthesizeable rtl (VHDL) design properly configured by means of a set of parameters allowing to specify peculiar behaviors (i.e. QoS) and some HW characteristics (i.e. IFs size, FIFOs size, etc.)

DDCM Main features

- 4 clock domains (STAC, registers, phy transmitter/receiver)
- Safe behavior with respect to clocks switch-off sequence (clocks safe switch-off sequence analysis carried out).
- Configuration mode pins for reset configuration
- Registers programming module for on fly configuration
    - 1/2/4/8 bytes operations with no byteenables
    - Programming allowed only before traffic start
    - Error in case of out of range address and unsupported opcode
- Optional retiming stages at STNoC interface
- Credit based flow control between DDCM transmitter in die #1 and DDCM receiver in die #2
- Virtual wires to transport asynchronous signals (interrupts, power down handshake, others) between dice, organized in up to 5 bundles
- Possibility to select "every cycle" as sampling rate for the virtual wires bundles.
- Fixed segment size (80 bits payload + 10 bits header) for data transfers
- Dynamically variable segment size for virtual wires and credits to optimize bandwidth consumption at physical level
- SW configurable Store & forward policy in targets request FIFOs, Store & forward policy never applied by initiators response FIFOs
- QoS: programmable fixed priority, programmable LRA algorithm, programmable bandwidth limiters
- 16/8 bits PHY working in both Single/Double Clock Edge (SCE/DCE) mode
- Frequency conversion between PHY adapter and PHY (for both transmitter and receiver)
- External PHY data driving capability via dedicated test interface for debugging purpose
- Support of DFT debug methodology
- Support of security encoder/decoder for data encryption at physical level
- Tolerance to phyt bubbles for safe data transport in case of slow send
- Activity driven clock-gating to save dynamic power

DDCM Technology

The block has been synthesized exploiting 32nm CMOS technology. A new synthesis at 28nm is forecasted in coming weeks. A 20% area saving is expected.

DDCM Implementation data

- Area
  - 307.042,89 μm^2
  - 289.664 gates-equivalent (around 300 Kgates)
  - 2.277 pins
- Timing
  - Clock in 200-600 MHz range (PLL in 400-1200 MHz
  - Up to 500 MHz internal operation frequency
    - 500 MHz with 16 elements FIFOs
    - 470 MHz with 128 elements FIFOs
  - Up to 450 MHz external operation frequency, limited by FIFOs size, extensible via retiming stages
    - 450 MHz with 16 elements FIFOs
    - 400 MHz with 128 elements FIFOs
  - 400/450 MHz operation frequency on Phy clock - 266/300/333/400/450 on System clock

Qualification

- VHDL functional verification: all tests passed
- Netlist functional verification: all tests passed
- Detailed Spyglass checks: no violations
- Code coverage: 100% (with justifications) code coverage
- Certitude analysis: no violations

7. Conclusion

In this document, the definitions of the devices comprising the plasmonic transceivers of the interconnect system were reported. In continuation of this report, the system simulations are about to begin, so that targeted system specifications and device specifications converge. At this point, there are challenges to be overcome, for example, the amplifier consumption is projected to be too high and the same goes for the photodetector delay. In the coming months, a major focus for the NAVOLCHI consortium will be on the aforementioned convergence.

8. References

[1] G. L. Li, X. Z. Zheng, J. Lexau, Y. Luo, H. Thacker, T. Pinguet, P. Dong, D. Z. Feng, S. R. Liao, R. Shafiiha, M. Asghari, J. Yao, J. Shi, I. N. Shubin, D. Patil, F. Liu, K. Raj, R. Ho, J. E. Cunningham, and A. V. Krishnamoorthy, "Ultralow-power silicon photonic interconnect for high-performance computing systems," Optoelectronic Interconnects and Component Integration IX7607, 760703 (2010).

[2] The 50G Silicon Photonics Link, Intel White paper, July 2010

[3] Texas Instruments Chip-to-Chip Link (C2C), http://www.arteris.com/c2c_chip-to-chip_for_DRAM_memory_sharing

[4] MIPI Alliance, http://www.mipi.org/

[5] V. Dolores-Calzadilla, *et al.*, "Towards plasmonic lasers for optical interconnects", IEEE Proceedings of the 14th International Conference on Optical Transparent Networks, 2012.