Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Technoeconomical evaluation with respect to energy efficiency and power consumption

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Executive Summary

This document presents a technical evaluation of chip interconnects with respect to the bandwidth density and power consumption. The implemented plasmonic-based architecture is evaluated and compared against alternative technologies like photonic and electronic interconnects. The comparison study is based on the latest data available from NAVOLCHI partners and literature, and is divided in two sections: In the first section, a comparison between conventional electronic CMOS, photonic and the Navolchi project interconnect approach is attempted, on the fields of energy efficiency and implementation details, at present and up to a long term time scale. In the second section, the comparison is specified at the device module level of an interconnect system, for both active (transmitters, receivers) and passive modules (waveguides, couplers), in terms of bandwidth density and energy efficiency.

Contents

1. Introduction

In nowadays, Data Centers (DC) and High Performance Computing (HPC) systems are experiencing limitations in terms of power consumption reduction. High Performance Computing (HPC) and Data Centers (DC) applications require more and more interconnection bandwidth, for less power dissipation, and smaller chip dimensions. It seems difficult for conventional CMOS-based electronic interconnects to satisfy the future interconnect requirements of an Exascale system, and hence, researchers are seeking for other interconnect technologies, in order to overcome the forthcoming limitations, such as optical and plasmonic technology.

A comparison between the aforementioned interconnect technologies and their possible future trends is attempted, to find out which technologies are more appropriate for implementing future high speed and energy efficient on-chip and off-chip interconnects. This is the focus of this report, which is based on the latest data available from NAVOLCHI partners and literature, and it is divided in two sections: In the first section, Navolchi project, interconnect approach will be compared with conventional electronic CMOS, and photonic interconnect technologies, on the fields of energy efficiency and implementation details, at present, and up to a long term time scale. In the second section, the comparison is specified at the device module level of an interconnect system, namely transmitters, receivers and interconnection means, in terms of bandwidth density and energy efficiency, and their potentials are considered as well, at the present and up to a long term time scale.

2. Summary comparison of conventional electronic, photonic and the Navolchi interconnect

In this section a comparison between conventional electronic CMOS, photonic and the Navolchi project interconnect approach is attempted, on the fields of energy efficiency and implementation simplicity, based on current state of the art data and the projected ones according to relevant roadmap predictions coming from giant industry leaders in

the interconnect market: specifically IBM and ST-Microelectronics [1],[2],[3]. Current and projected values between these two corporations are in compliance with each other, hence giving in numbers the trends of interconnection technology. Concerning the conventional CMOS interconnect technology, energy efficiency in pJ/bit estimations are based on current and projected values of the most updated ITRS tables [4]. Following the work by Miller [5]-[8], we have also assumed that interconnect power is approximately 20% of the total chip power.

<table>
<tr><th rowspan="2">Year</th><th rowspan="2">Node techn. (nm)</th><th colspan="4">Energy efficiency in pJ/bit</th><th colspan="2">Optical technology roadmap</th></tr>
<tr><th>Navolchi (hybrid)</th><th>IBM optical</th><th>STmicro optical</th><th>CMOS convent. (ITRS projected)</th><th>Navolchi (hybrid)</th><th>Optical</th></tr>
<tr><td>2013</td><td>28</td><td>10-20</td><td>‹25</td><td>15</td><td>30-40</td><td rowspan="3">Cu/VCSEL for Backplane</td><td>AOC and VCSEL Backplane</td></tr>
<tr><td>2015</td><td>24</td><td></td><td></td><td></td><td></td><td>Si Ph for Backplane</td></tr>
<tr><td>2016/2017</td><td>22/20</td><td>~5</td><td>5</td><td>4.4</td><td>11-8</td><td rowspan="2">Si Ph for interposer and Board</td></tr>
<tr><td>2018</td><td>18</td><td></td><td></td><td></td><td></td><td rowspan="2">Cu/VCSEL and Si Ph. for Backplane</td></tr>
<tr><td>2019/2020</td><td>17/15</td><td>~1-2</td><td>~1</td><td>‹1.7</td><td>4.5-3</td><td rowspan="4">Si Ph on chip</td></tr>
<tr><td>2021-2024</td><td>14-11</td><td></td><td></td><td></td><td></td><td>Cu/VCSEL and Si Ph. for Board</td></tr>
<tr><td>2025</td><td>10</td><td>~0.5</td><td></td><td></td><td>1.3</td><td rowspan="2">Si Ph. Onto chip</td></tr>
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Table 1 – Energy comparison of different chip interconnect technologies

The two aforementioned interconnect technologies will be compared with the Navolchi project interconnect technology roadmap, which combines conventional optical technology for interconnecting the two chips, with plasmon based active modules, such as directly modulated sources, or modulator, for transmitters(chip 1), and plasmonic QD

based photodetectors(chip 2) [9]. Concerning Navolchi project, the source for the roadmap information comes Navolchi Work Package 2, IMEC optical interconnect program - confidential. The results are summarized in Table 1.Concerning energy dissipation performance, it seems that the Navolchi interconnect keeps in pace with the photonic interconnect value range at the moment and for the long term, as expected, since both are based on common and promising silicon photonic technology. Conventional CMOS interconnect, as expected, seems to be a bit behind from its two technology competitors, in terms of energy dissipation downscaling. Plasmon based interconnect will be compared with an all optical in the next section at chip module level.

3. On/off chip interconnect comparison at the device level

In this section we attempt to compare in terms of energy efficiency, each device module that a typical interconnect consists of (see Figure 1), namely a transmitter, which can be either a directly modulated laser or an external modulator, a receiver which apart from the photodetector, may or may not include an amplifier, and waveguide accompanied with appropriate couplers as connection means.

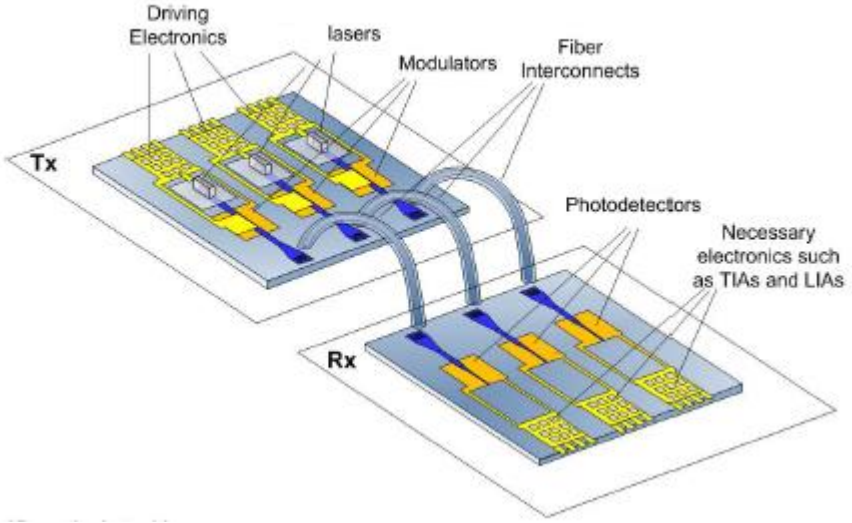

Figure 1 - 2D typical interconnect structure [Source: Navolchiproject http://www.imt.kit.edu/projects/navolchi/]

Miller [5]-[8]and other researchers [10]-[13], have set the energy targets for the optical interconnect technology in order to become much more competitive than conventional

interconnects in future years. Of course these projections and estimations are based on assumptions for the Byte/FLOP ratio or the I/O chip bandwidth or the % percentage of the interconnect power of the total chip power dissipated, and may slightly differ with each other, but they certainly indicate the trend and the global energy target to be achieved , for the future. Specifically, past researches have considered that in a long, seven year time scale, in order to be competitive with conventional interconnects, total interconnect system energy should be within 50-170fJ/bit for off-chip interconnects and 10-50fJ/bit for on-chip, while device interconnect energy for off-chip should be within 10-50fJ/bit, and within 2-10fJ/bit for on chip respectively. For this purpose, we have gathered in tables, the most recent references from the literature, related with energy performance of chip interconnects, classified at the device level, for both competitive optical technologies; photonics and plasmonics. Since energy efficiency is directly related to the bit rate, the maximum operating bit rate, that each device can achieve, is of great importance, and it is considered as well in the analysis summarized in the following tables. Moreover, for each active chip interconnect module, active area dimensions have been considered, since, for a given bit rate they are directly related to module's bandwidth density, an important parameter to be taken for granted as well. We have to state that all references are based on experimental research work.

a. Directly Modulated Lasers. For a directly modulated laser, a few tens of femtojoule per bit energy for off-chip, let alone less than ten fJoule for on-chip interconnect power, is quite low to be achieved. Vertical-Cavity Surface-Emitting Lasers (VCSELs), as can be seen from the table below, can usually reach more or less a few hundred fJ per bit energies, with the best performance lying at 56fj/bit at 25Gbps [14], and hence they cannot keep up with future on-chip energy requirements, despite the fact they are considered to be state of the art transmitters for board to board interconnections nowadays. DFB laser structures are far less energy efficient with energies at a few pJ per bit, so they are out of the question, as well[15]. Silicon nanophotonics technology is more promising and can achieve transmitter energies around few tens of fJ/bit [13]. Photonic crystal nanocavity lasers (or even LEDs) with or without quantum dot gain region for amplification, or silicon nanowire laser structures may stand a chance to be possible on chip transmitters for the future energy requirements, with energies from a few fJoules up to 10fJ/bit, as can be seen in the table. LEAP (lambda-

scale embedded active-region photonic-crystal) lasers of the photonic crystal family, is considered the most promising directly modulated transmitter, energy efficient solution for meeting future energy requirements [16]. Moreover they can be fabricated with photonic crystal diodes on the same wafer, thus creating on chip optical links consisting of LEAP laser transmitters and PhC photodiodes receivers [17]. Plasmonics may play a key role in the case of directly modulated transmitters, with nanolasers with metallo-dielectric cavities, or nano LED structures consuming power at the microwatt region, but at modest operating rates of up to a couple tens of Gbps [36]. SPACER technology (surface plasmon amplification by stimulated emission currents and power) has been adopted in order to compensate for the lossy plasmonic material.

b. External Modulation Sources. By using modulators instead of a directly modulated source low energies can be achieved because, unlike lasers, modulators do not have a threshold that could limit the minimum operating energy. Hence, externally modulated sources are more promising transmitter candidates than directly modulated laser sources, for future on chip interconnections. There are two main modulator classes, the interferometric MZ structures, that rely on changes of the relative phase of the interfering beams by changing the refractive index, that lead to changes of the output power, and EAM, that rely on changes of the optical absorption in a semiconductor structure by applying voltage to it. Typical MZ interferometer modulators require long arm lengths in order to achieve strong refractive index changes, so they require large footprints. One solution would be the use of other materials with higher refractive index changes, such as electrooptic polymers (EOP) [37]. Another alternative would be the use of ring resonators in order to enhance the effect of changing the refractive index in only a smaller length of material such as low-energy, high-speed silicon ring or disk resonators.

Table 2: Photonic and Plasmonic Directly Modulated Sources.

Energy/Power consumption	Description	Bit rate/BW	Area	Reference
77fJ/bit (el) 56 fJ/bit (dissipated)	VCSEL	25Gbps	20-30um	[14]
83/117fJ/bit (el) 569/99 fJ/bit	VCSEL	17/25Gbps	20-30um	[18], [19]

(dissipated)				
140fJ/bit(el) 107 fJ/bit (dissipated)	VSCEL	34Gbps	20-30um	[20]
158fJ/bit(el) 108 fJ/bit (dissipated)	VCSEL	40Gbps	20-30um	[21]
180fJ/bit(el) 140 fJ/bit (dissipated)	VCSEL	10Gbps	20-30um	[22]
203fJ/bit(el) 177 fJ/bit (dissipated)	VCSEL	38Gbps	20-30um	[23]
287fJ/bit(el) 233 fJ/bit (dissipated)	VCSEL	85Gbps	20-30um	[24]
470fJ/bit(el) 330 fJ/bit (dissipated)	VCSEL	32Gbps	20-30um	[25]
750fj/bit	Hybrid III-V (InP)on SOI	NA	$5um^2$	[26]
800fj/bit	hybrid III-V on Si	NA	NA	[27]
750/500fj/bit	Hybrid III-V (InP) on Si	40/25.8Gbps	$96um^2$	[28]
82.5fj/bit	Microdisk InP	NA	$7.5um^2$	[29]
13fJ/bit	Photonic crystal nanocavity laser w/wo QD	5Ghz	NA	[30]
8.76fJ/bit or 175.2 μW	InGaAsP/InP BH PhC laser	20Gbps	dimensions: 5.0 x 0.3 x 0.15 μm^3	[31], [33]
4.4fJ/bit-44uW	PhC laser LEAP	10Gbps	dimensions: 16um x7um	[32]
0.25 fJ/bit 2.5uW	Photonic Crystal Nanocavity LED with QD	10Ghz	NA	[34], [35]
1.15fj/bit	El driven Plasmonic nanoLED	0.1Gbps	80nm x 4um	[36]

*For VCSEL concerning energy estimation: Pel = V•I, is the electrical continuous wave power, V and I are the direct current (DC) operating voltage and bias current of the VCSEL, Pdiss = Pel – Poptical is the dissipated power, Poptical is the total optical output power. Concerning active area dimensions, their typical actual diameter ranges from 20-30um.

Table 3: Photonic and Plasmonic Modulators.

Energy/Power consumption	Description	Bit rate/BW	Area	Reference
640fj/bit	SOH EOP MZM polymer	112Gbps (56Gbps error free)	length 1.5 mm w=140nm	[38]
94.4fj/bit	SOI MZI EOP polymer	10Gbps	300um length width 320nm	[39]
100fJ/bit 2.5mW	Ge FKE EAM	25 Gbps	$1.0 \times 45um^2$	[40]
50fJ/bit	Ge Si FKE EAM	1.2 Gbps	30 um2	[41]
7.9fj/bit	Silicon microring	1Gbps	$20um^2$	[42]

3fj/bit	Silicon microdisk	12.5Gbps	10 um^2	[43]
1.6fj/bit	(SOH) modulator	12.5Gbps	1mm length 160nm width	[44]
0.75fJ/bit 500uW	Ge on Si	>7Gbps	footprint of 8 um^2	[45]
1.1fj/bit	GaAs PhC EOM	100Ghz	NA	[46]
25fj/bit	All plasmonic EOP(Navolchi)	54Gbps	length 5um	[47]
18fJ/bit	EOP polymer(Navolchi)	40Gbps	29umx29um	[48]
20fJ/bit	Plasmonic MZ (Navolchi)	72Gbps	10umx1.5um	[49]

* For modulators concerning energy matter, they all consider dynamic switching energy.

c. Photodetectors. Photodetector's received optical energy is directly related with transmitters' optical output power and the total link loss power budget, which includes total link attenuation, coupling losses and eventually, a power margin. Hence, for 10 fJ/bit transmitted optical energies, the received optical energy would be ~1 fJ/bit(1eV photons) in a reasonable optical system allowing for various losses [5]. So we are targeting for photodetectors with total capacitance of a few fFarads at most, in order to compete as possible receivers for future on chip interconnections. It is known that useful features for photodetectors are large responsivity, at low dark current and capacitance and high sensitivity and bandwidth. Typical photodetector structures are P-N, or PIN heterojunctions built by semiconductor materials, such as Si, Ge, and III-V material, and Schottky structures. For low power consumption and high speed circuits, the goal for the detector is to reduce its capacitance by shrinking its size into the nanoscale. Silicon photonics at nanoscale (nanophotonics), has main representative photodetector structures, Ge based detectors built on silicon substrate forming either PIN or APD structures. The latter has better sensitivity than the p-i-n type detectors and exhibit larger gain bandwidth product, and hence gives better performances.

Plasmonic-based photodetectors can be categorized into two types, depending on the way they accept the optical data. In the first detector type, optical data are converted to plasmonic and the challenge is to match the large photonic mode to

a tiny plasmonic one before it can be absorbed and detected later on. This can be achieved with the use of apertures to confine optical beams and tapered nanometallic waveguides, with incredible performances, concerning energy efficiency. The second detector type is based on plasmonic integrated circuits, and a typical structure is a crossing of a metal and a semiconductor Ge nanowire to form a Schottky junction. Ge particles absorb incoming optical data, creating electron-hole pairs, which can be, later on, extracted by the plasmon polariton waveguide, allowing for a densely integrated design.

As can be seen from the table below, plasmonic detector schemes can be much more energy efficient than nanophotonics competitors providing energies at the attojoule levels. Plasmonic detector offer multiple advantages such as high integration densities due to their ultra small sizes, and low device capacitance leading to ultra high bandwidth operation, and ultra low energies.

Table 4: Photonic and Plasmonic Detectors.

Energy/Power consumption	Description	Bit rate/BW	Area	Reference
33fJ/bit-100uW	Ge PD	3Gbps	Length 40um	[52]
2.4fJ/bit	Ge PD on Si	40Gbps	Length 30um	[53]
2 fJ/bit	Ge APD in Si	10Gbps	Diameter 30um	[53]
0.4fj/bit	Inp/InGaAs PD	10Gbps	3.4-µm-long	[55]
5aJ/bit	Nanometallic Antenna PD	NA	Active volume 0.00072um3	[56]
10-100aJ/bit	Integrated plasmonic Ge photodetector	50Gbps	length 100nm	[57]
80aj/bit	Au Nanoantenna into GaAs NW	NA	12µm long diameter 70 nm.	[58]

d. Passive devices: waveguides and couplers. Table 5, shows Silicon based and Plasmonic based waveguides along with their attenuation losses. Table 6 shows coupling losses of a conventional coupler, and a coupler used for photonic to plasmonic mode conversion. It is obvious that plasmonic waveguide material is too lossy with propagation losses in the order of dB/um, while their photonic counterpants, are in the order of dB/cm. A solution, as mentioned, would be to

compensate loss with gain, using either nanoparticles (QD with gain), or SPASER mechanism. These cases of active waveguiding are not included in Table 5. The maximum interconnection length that can be supported by plasmonic waveguides, before become too lossy, is around 100um [59], which is too low for supporting global interconnections. The most appropriate link scenario, is the hybrid link, that consists of energy-efficient high-speed plasmonic modulator in conjunction with conventional photonic waveguides which should be used instead of plasmonic ones. In [59] it has been shown that hybrid channels are clearly more energy efficient than plasmonic channels at any length, and become more energy efficient than electrical from 200 um which means that they can be used even for the shortest type of on chip interconnects. The only additional loss they require is the photonic to plasmonic mode conversion coupling and vice versa, which as can be seen in Table 6, is very low, adding a few dBs more on the total link budget.

Table 5: Photonic and Plasmonic Waveguides.

Material	Attenuation	Reference
silicon core on insulator (SOI)	0.5dB/cm	[60]
silicon core on insulator (SOI)	1.4-4.5dB/cm	[61]
plasmonic(M-I-Si.I-M)	0.28-0.3dB/um	[62]
Slot-line	3.0733 dB/μm	[63]
Hybrid plasmonic	0.01-0.22dB/um	[63]

Table 6:Couplers.

Description	Coupling loss	Reference
Fiber to Si waveguide	< 1dB	[64]
photonic to plasmonic mode conversion	1.1dB	[65]
coupling losses per Si-to-DLSPP interface	2.5 dB	[66]

Figures 2a-2c, show minimum and maximum energy efficiency values, for each interconnect device module (laser sources, modulators and detectors) respectively, specifying their implementation technology as well. Minimum and maximum values can be seen in labels on each column in fj/bit unit, though they are represented in axes in logarithmic scale for better value fitting. Concerning directly modulated sources, as can

be seen from figure 2a, the best energy performance comes from InP based photonic crystal nanocavity, or LEAP lasers with energies from a few fJoules up to 10fJ/bit, hence capable of meeting future energy requirements. Their energy performance can almost compete with plasmonic nano LED structures with energies just a few fJoules. VCSELs and hybrid III-V on Si laser structures, as can be seen from figure 2a, are far less energy efficient with energies more or less a few hundred fjoules, with the best performance lying at sub hundred fjoules [14], and hence they cannot be considered capable of meeting future on-chip energy requirements, though they are state of the art transmitters for board to board interconnections nowadays.

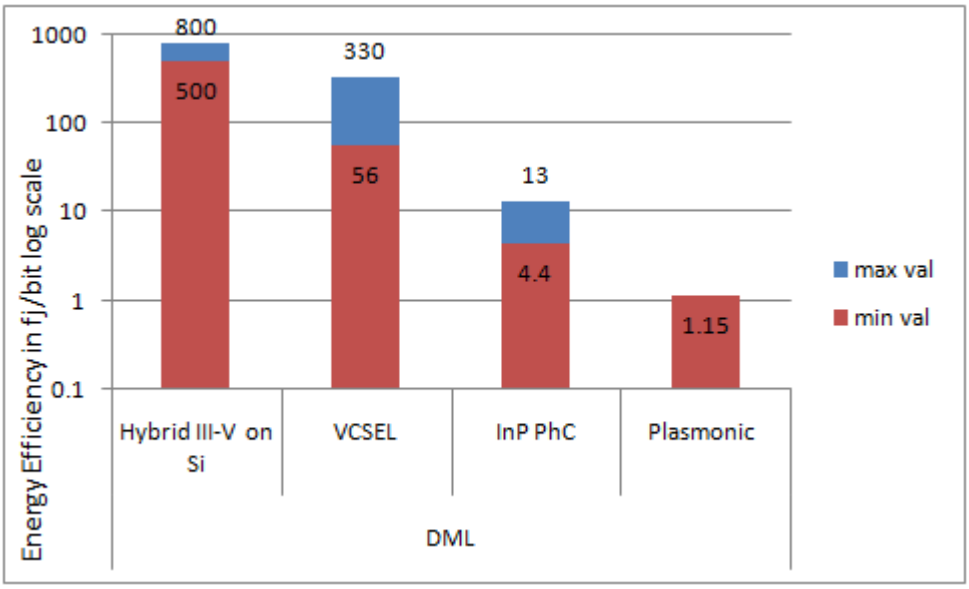

Fig. 2a – Chip interconnect energy efficiency for directly modulated sources

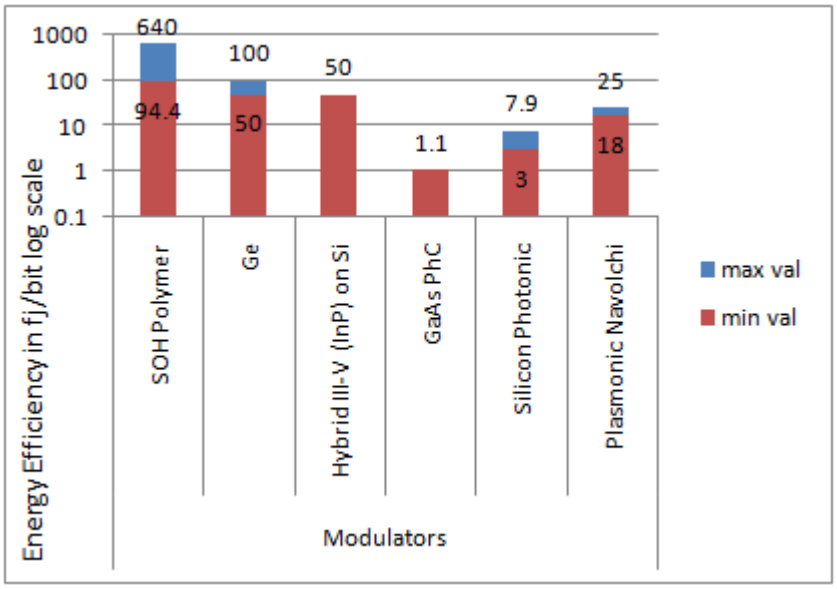

Fig. 2b – Chip interconnect energy efficiency for modulators

Concerning modulators, as can be seen from figure 2b, the best energy performance comes from nano scale Silicon Photonics based modulators with energy performance ranging from a few fJoules up to 10fjoules. However this is not always the case, since, other photonic modulator structure energies usually vary from a few hundred of fJ's up to sub hundred fJ's, such as Hybrid InP on silicon, or Ge on silicon, or silicon organic polymer modulator structures. Navolchi plasmonic modulators really stand a good energy performance lying at a few tens of fJ's, slightly above the best performance of photonic modulators.

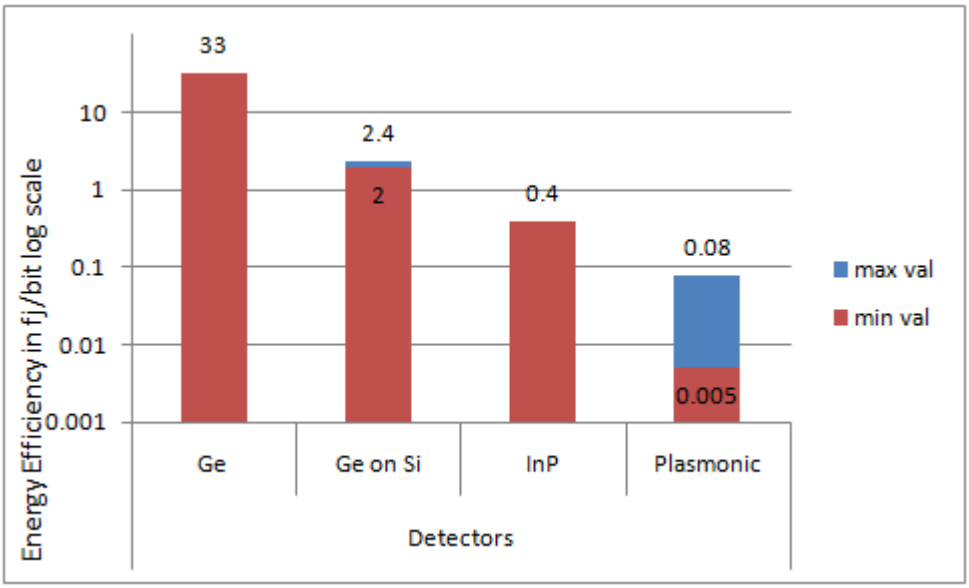

Fig. 2c – Chip interconnect energy efficiency for photodetectors

Concerning receiver side, as one can see from figure 2c, energy performance superiority of a Plasmonic photodetectors (integrated Ge, or nanoantenna structures), is crystal clear, compared with a typical Ge photodetector on Si or even enhanced with avalanche mechanism. Plasmonic integrated Ge photodetector[57] total parasitic capacitance lies between 10 and 100 aF, thus giving energies between 10 and 100 aJ, respectively, considering 1V drive swing voltage, which are orders of magnitude less than the aforementioned energies of a typical Ge on Si photodetector.

As can be deducted from figures 2a-2c, the bottom line is that, with the exception of photodetector energy performance comparison, photonic based chip inerconnect modules are considered to be comparable to plasmonic based ones in terms of energy efficiency. However plasmonic based devices strong point is their relatively ultra small dimensions leading to high integration densities, and with their low device capacitance allowing for ultra high bandwidth operation. It is then worth it, comparing chip module bandwidth density versus energy efficiency, to observe another point of comparison view among the aforementioned technologies. Figures 3a-3c, show energy efficiency versus bandwidth density values, for each interconnect device module (laser sources, modulators and detectors) respectively, specifying their implementation technology as well.

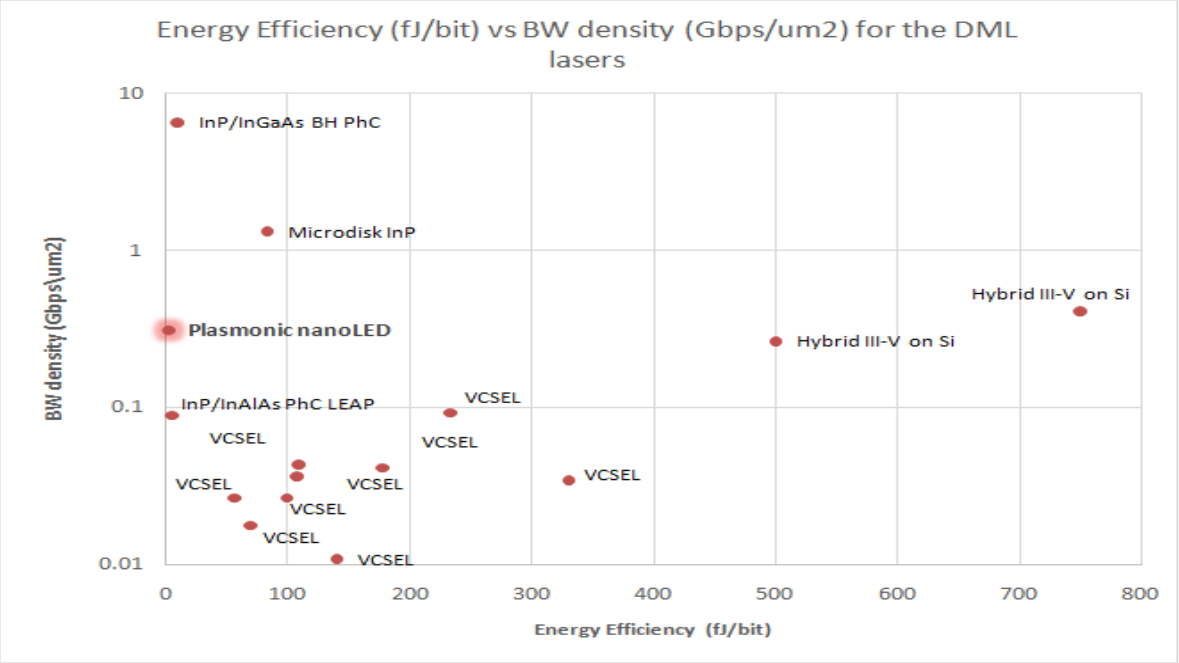

Fig. 3a –Energy efficiency vs BW density for directly modulated sources

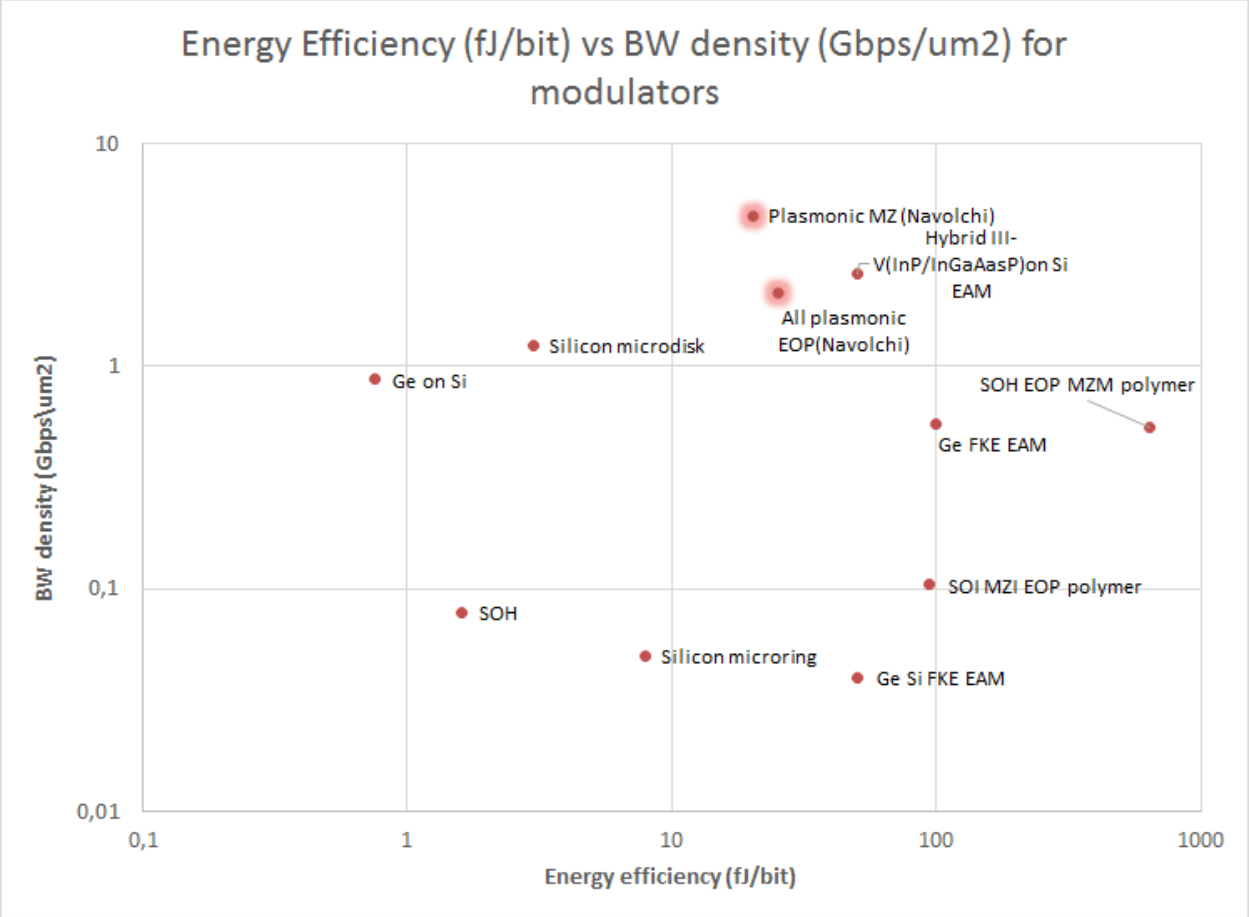

Fig. 3b –Energy efficiency vs BW density for modulators

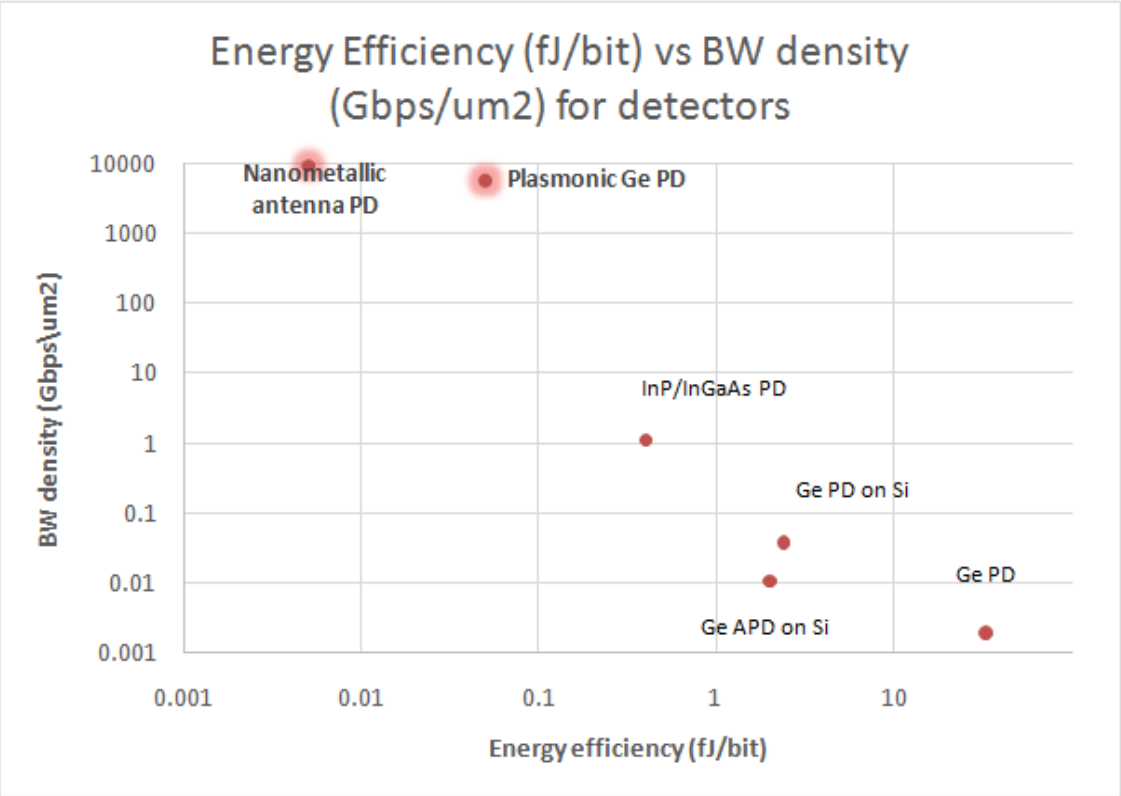

Fig. 3c –Energy efficiency vs BW density for photodetectors

As can be seen in figures 3a-3c best combined performances should be considered those that have the greatest bandwidth density (placed at the highest possible level on y axis-BW density), while at the same time have the lowest energy consumption (placed at the leftmost level of x axis – energy efficiency). Concerning directly modulated sources, as can be seen from figure 3a, the best combined performance comes from InP based photonic crystal nanocavity, again competing with plasmonic nano LED structures. Concerning modulators, as can be seen from figure 3b, the best combined performance comes from Hybrid Plasmonic structures beating nano scale Silicon Photonics, as the former are placed higher than the latter, due to their clear superiority on the grounds of BW density, while their energy performance is more or less about the same. Navolchi modulators are placed higher than nano scale Silicon Photonics as well, again prooving their superiority in terms of BW efficiency, while their energy performance is slightly worse than silicon nanophotonics. Finally, the clearest combined superiority by far, comes out from figure 3c, where one may notices quite clearly the combined superior performance of plasmonic photodetectors against conventional Ge photodetectors on both terms of energy efficiency and bandwidth density.

4. Conclusions

A comparison among conventional CMOS, photonic and plasmonic chip interconnect technologies, in terms of bandwidth density, and energy efficiency, has been attempted, based on the latest data available from NAVOLCHI partners and literature. These three technologies were compared at interconnect system level and at device chip module of the interconnect system level, as well. The comparison showed that, among conventional CMOS, photonic and plasmonic technologies, in terms of energy dissipation, both photonic and plasmonic solutions can surely implement energy efficient chip module devices, and on/off chip interconnects that could meet future prospects.

However as the more thorough, bandwidth density versus energy efficiency combined comparison showed, plasmonic based devices have another strong key point that prooves their superiority against photonic nanoscale devices, and that is their active region ultra small dimensions. That advantage leads to high integration densities, and low device capacitance allowing for ultra high bandwidth operation. At the device module level, and specifically concerning direct modulated sources, photonic crystal nanocavity lasers or plasmon nano LED structures may well be considered as chip transmitters that would without a doubt, meet the future energy requirements, and bandwidth density matters as well.

However, an externally modulated transmitter is considered a more preferable and energy efficient solution than directly modulated sources, since, silicon micro- and nano-scale photonic modulators, or plasmonic modulators (hybrid or plain) are considered a more mature solution and they can reach energies, from a few fjoules up to a few tens of fjoules, thus adequately supporting energy efficient transmission for future on chip interconnections. Yet, in between photonic and plasmonic modulator structures, the latter is preferable to the former, since they can reach ultra-high levels of bandwidth density, and hence they may certainly be more suitable for integration purposes.

Finally at the receiver side, in order to have low power consumption and high speed circuits, the ultimate target for the detector is to reduce its capacitance by shrinking its size, thus increasing its bandwidth density. Conventional Ge based detectors built on

silicon substrate forming PIN or APD structures can be adequately considered, as energy efficient receivers for future interconnect demands. However, plasmonic detector schemes can be even more energy efficient modules, reaching energies at attojoule levels, with capacitance at attofarad levels (one order of magnitude lower than photonics) and that makes them uncompetitive energy efficient chip modules, with greatest integration potential.

5. References

[1] Benner IBM "Optical interconnect opportunities in supercomputers and high end computing" OFC 2012

[2] Zuffada "Low cost silicon photonics technology platform: plans perspectives and roadmap" ECOC 2013

[3] Zuffada "Vision on silicon photonics for efficient data communications" Photonics 21 WG6 Workshop 2013

[4] http://www.itrs.net/

[5] Miller "Device requirements for optical interconnects to silicon chips" IEEE proc. Vol.97, No 7, July 2009

[6] Miller "optical interconnects" OFC 2010

[7] Miller "Optical interconnects to electronic chips" Applied Optics vol.49, No 25, Sept. 2010

[8] Miller "Low energy optoelectronics for interconnects" INC 10, May 2014

[9] http://www.imt.kit.edu/projects/navolchi/

[10] Tucker "Green optical communications-Part I: Energy limitations in Transport" IEEE, J. of Sel. Topics in Quant. Communications, 2010

[11] Tucker "Green optical communications-Part II: Energy limitations in Networks" IEEE, J. of Sel. Topics in Quant. Communications, 2010

[12] Tucker et al "Energy consumption and energy density in optical and electronic signal processing" IEEE Photonics Journal, vol 3, No 5, Oct. 2011

[13] S. Manipatruni "Device scaling considerations for nanophotonic CMOS global interconnects" IEEE, J. of Sel. Topics in Quant. Communications, vol 19, No 2, March/April 2013

[14] P. Moser, J.A. Lott, P. Wolf, G. Larisch, H. Li, N.N. Ledentsov, and D. Bimberg: 56 fJ dissipated energy per bit of oxide-confined 850 nm VCSELs operating at 25 Gbit/s, Electron. Lett., vol. 48, pp. 1292-1293, Sep. 2012

[15] S. Matsuo, T. Fujii, K. Hasebe, K. Takeda, T. Sato, and T. Kakitsuka, "Directly modulated buried heterostructure DFB laser on SiO/Si substrate fabricated by regrowth of InP using bonded active layer," Opt. Express 22(10), 12139–12147 (2014).

[16] K. Takeda, et al “Heterogeneously integrated photonic-crystal lasers on silicon for on/off chip optical interconnects” OSA, Vol. 22, No. 26, 29 Dec 2014

[17] K. Takeda, et al “Integrated On-Chip Optical Links Using Photonic-Crystal Lasers and Photodetectors with Current Blocking Trenches,” in Optical Fiber Communication Conference (OFC), 2013 OSA Technical Digest Series (Optical Society of America, 2013), paper OM2J.5.

[18] W. Hofmann , P. Moser and D. Bimberg “”Energy-Efficient VCSELs for Interconnects”” IEEE ph. journal, vol. 4, no. 2, April 2011

[19] P. Moser, et al ”81 fJ/bit energy to-data ratio of 850 nm vertical-cavity surface-emitting lasers for optical interconnects” Appl. Phys. Lett., vol. 98, no. 23,, Jun. 2011.

[20] J.-W. Shi, J.-C. Yan, J.-M. Wun, J.A. Chen, and Y.Y. Yang: Oxide-relief and Zn-diffusion 850-nm vertical-cavity surface-emitting lasers with extremely low energy-to-data-rate ratios for 40 Gbit/s operations, IEEE J. of Sel. Top. in Quantum Electron., vol. 19, pp. 7900208, Mar.-Apr. 2013

[21] P. Wolf, P. Moser, G. Larisch, H. Li, J.A. Lott, and D. Bimberg: Energy efficient 40 Gbit/s transmission with 850 nm VCSELs at 108 fJ/bit dissipated heat, Electron. Lett., vol. 49, pp. 666–667, May 2013

[22] S Imai et al “Recorded low power dissipation in highly reliable 1060-nm VCSELs for green optical interconnection” IEEE J. Sel. Topics Quantum Electron., vol. 17, no. 6, pp. 1614–1620, Nov./Dec.2011

[23] H. Li, H., P. Wolf, P. Moser, G. Larisch, A. Mutig, J.A. Lott, and D. Bimberg: Energy-efficient and temperature-stable oxide-confined 980 nm VCSELs operating error-free at 38 Gbit/s at 85°C, Electron. Lett., vol. 50, pp. 103-105, Jan. 2014

[24] P. Moser et al “ 85 ^{0}C error-free operation at 38Gbps of oxide-confined 980-nm vertical-cavity surface-emitting lasers” Appl. Phys. Lett., vol. 100, no. 8, Feb. 2012.

[25] P. Westbergh et al “ 32 Gbit/s multimode fibre transmission using high-speed, low current density 850 nm VCSEL “ Electron. Lett., vol. 45, no. 7, pp. 366–368, March 2009.

[26] Y. Halioua et al “Hybrid III-V semiconductor/silicon nanolaser” Optics Express 9 May 2011 / Vol. 19, No. 10 OSA

[27] S. Chung et al “Low-Energy-Consumption Hybrid Lasers for Silicon Photonics” paper Mo.C4.1, ICTON 2012

[28] Matsuo, S. et al. “Directly modulated buried heterostructure DFB laser on SiO2/Si substrate fabricated by regrowth of InP using bonded active layer,” Opt. Express 22, 12139–12147, 2014.

[29] J. Van Campenhout et al “Electrically pumped InP-based microdisk lasers integrated with a nanophotonic silicon- on-insulator waveguide circuit” Optics Express 28 May 2007 / Vol. 15, No. 11 OSA

[30] Matsuo, S. et al. High-speed ultracompact buried heterostructure photonic crystal laser with 13fJ of energy consumed per bit transmitted. Nature Photon. 4, 648-654 (2010)

[31] Matsuo, S. et al. “20-Gbit/s directly modulated photonic crystal nanocavity laser with ultra-low power consumption” Optics Express, Vol. 19, Issue 3, pp. 2242-2250 (2011)

[32] K. Takeda, et al “Few fJ/bit data transmissions using directly modulated lambda scale embedded active region photonic crystal lasers”, Nat. Photon 7, 569- 575 (2013).

[33] S Matsuo et al “20-Gbit/s directly modulated buried heterostructure photonic crystal laser with 8.76-fJ/bit operating energy” ECOC 2010

[34] G. Shambat et al “Electrically Driven Photonic Crystal Nanocavity Devices” IEEE J of Sel Topicsin Q Electronics, vol. 18, No. 6, November/December 2012

[35] Vuckovic et al “Ultra-Low Threshold and High Speed Electrically Driven Photonic Crystal Nanocavity Lasers and LEDs” CTu1N.5 CLEO Technical Digest © OSA 2012

[36] Huang “Electrically driven subwavelength optical nanocircuits” NATURE PHOTONICS Vol 8, March 2014

[37] X. Zhang et al “Polymer based hybrid integrated photonic devices for silicon on chip modulation and board level optical interconnects” IEEE, J. of Sel. Topics in Quant. Communications, vol 19, No 6, Nov/Dec 2013

[38] D. Korn et al “Silicon-organic hybrid (SOH) IQ modulator using the linear electro-optic effect for transmitting 16QAM at 112 Gbit/s” Optics Express 3 June 2013 Vol. 21, No. 11 OSA

[39] X. Zhang et al “Broadband energy efficient optical modulation by hybrid integration of silicon nanophotonics and organic electrooptic polymer” Proc. SPIE 9368, Optical Interconnects XV, April 2015

[40] N. Feng, D. Feng, S. Liao, X. Wang, P. Dong, H. Liang, C.-C. Kung, W. Qian, J. Fong, R. Shafiiha, Y. Luo, J. Cunningham, A. V. Krishnamoorthy, and M. Asghari, “30GHz Ge electro-absorption modulator integrated with 3 μm silicon-on-insulator waveguide,” Opt. Express 19(8), 7062–7067 (2011).

[41] J. Liu, M. Beals, A. Pomerene, S. Bernardis, R. Sun, J. Cheng, L. C. Kimerling, and J. Michel, “Waveguide integrated, ultralow-energy GeSi electro-absorption modulators,” Nat. Photonics 2(7), 433–437 (2008).

[42] S. Manipatruni, K. Preston, L. Chen, and M. Lipson, “Ultra-low voltage, ultra-small mode volume silicon microring modulator,” Opt. Expr., vol. 18, no. 17, pp. 18235–18242, 2010.

[43] M. R. Watts, W. A. Zortman, D. C. Trotter, R. W. Young, and A. L. Lentine, “Vertical junction silicon microdisk modulators and switches,” Opt. Express 19(22), 21989–22003 (2011).

[44] R. Palmer et al “High-Speed Silicon-Organic Hybrid (SOH) Modulator with 1.6 fJ/bit and 180 pm/V In-Device Nonlinearity”ECOC 2013 Paper We.3.B.3 Sept London

[45] S. Ren, Y. Rong, S. A. Claussen, R. K. Schaevitz, T. I. Kamins, J. S. Harris, and D. A. B. Miller, “Ge/SiGe quantum well waveguide modulator monolithically integrated with SOI waveguides,” IEEE Photon. Technol. Lett. 24(6), 461–463 (2012).

[46] G Shambat et al “Ultra-low power fiber-coupled gallium arsenide photonic crystal cavity electro-optic modulator” Optics Express Vol. 19, Issue 8, pp. 7530-7536 (2011)

[47] Haffner et al “All-Plasmonic Mach-Zehnder Modulator Enabling Optical High-Speed Communication at the Microscale” Nature Photonics 9, pp 525–528 (2015)

[48] Melikyan et al “High speed plasmonic phase modulators” Nature Photonics letters vol.8, March 2014

[49] Haffner et al “High speed plasmonic MZ modulator in a waveguide” ECOC 2014

[50] Piccus” Silicon Plasmon Modulators: Breaking Photonic Limits” IEEE Photonics Society Newsletter December 2013

[51] Ye et al "λ -Size ITO and Graphene-Based Electro-Optic Modulators on SOI" IEEE J of Sel Topics in Quantum Electronics, vol 20, no. 4, July/August 2014

[52] L. Chen, K. Preston, S. Manipatruni, and M. Lipson, "Integrated GHz silicon photonic interconnect with micrometer-scale modulators and detectors," Opt. Express, vol. 17, pp. 15248–15256, 2009.

[53] L. Chen and M. Lipson, "Ultra-low capacitance and high speed germanium photodetectors on silicon," Opt. Expr., vol. 17, pp. 7901–7906, 2009

[54] Y. Kang "Monolithic Ge/Si Avalanche Photodiodes" Group IV Photonics, 2009. GFP '09. Paper WB6, 6th IEEE International Conference

[55] K Nozaki et al "InGaAs nano-photodetectors based on photonic crystal waveguide including ultracompact buried heterostructure" Optics Express 12 August 2013 Vol. 21, No. 16, OSA.

[56] L. Tang, S. E. Kocabas, S. Latif, A. K. Okyay, D.-S. Ly-Gagnon, K. C. Saraswat and D. A. B. Miller, "Nanometre-Scale Germanium Photodetector Enhanced by a Near-Infrared Dipole Antenna," Nature Photonics 2, 226 – 229 (2008)

[57] P. Wahl et al "Energy-per-Bit Limits in Plasmonic Integrated Photodetectors" IEEE J. of Sel. Topics in Q. el. Vol. 19, No 2, March/April 2013

[58] A. Casadei et al "Photonic-Plasmonic Coupling of GaAs Single Nanowires to Optical Nanoantennas" NanoLett. 2014, 14, pp 2271-2278

[59] Wassel et al "Opportunities and challenges of using plasmonic components in nanophotonic architectures" IEEE 2012

[60] Lo "Silicon Photonics Technologies for Monolithic Electronic-Photonic Integrated Circuit" ECS Transactions, 28 (1) 3-11 (2010)

[61] Ding "OIL: A Nano-photonics Optical Interconnect Library for a New Photonic Networks-on-Chip Architecture" SLIP'09, July 26-27, 2009, San Francisco, California, USA

[62] S. Zhu et al "CMOS-Compatible Silicon Nanoplasmonics for On-Chip Integration" World Academy of Science, Engineering and Technology Vol:6 2012-09-22

[63] Silicon and plasmonics-based nanophotonics for telecom and interconnects 2014 THYLEN

[64] J. Lu and J. Vukovic, "Objective-first design of high-efficiency, smallfootprint couplers between arbitrary nanophotonic waveguide modes," Opt. Expr., vol. 20, pp. 7221–7236, 2012

[65] C. Delacour, S. Blaize, P. Grosse, J. M. Fedeli, A. Bruyant, R. Salas-Montiel, G. Lerondel, and A. Chelnokov. Efficient directional coupling between silicon and copper plasmonic nanoslot waveguides: toward metaloxidesilicon nanophotonics. Nano Letters, 10(8):2922–2926, 2010

[66] Pleros et al "Tbps switching for optical interconnects using heterointegration of plasmonics and silicon photonics: The FP7 PLATON approach" ECOC 2012