Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Report on Modelling of the Modulator Structure

Deliverable no.:	D3.2
Due date:	10/31/2012
Actual Submission date:	10/31/2012
Authors:	KIT
Work package(s):	WP3
Distribution level:	RE[1] (NAVOLCHI Consortium)
Nature:	document, available online in the restricted area of the NAVOLCHI webpage

[1] **PU** = Public

PP = Restricted to other programme participants (including the Commission Services)

RE = Restricted to a group specified by the consortium (including the Commission Services)

CO = Confidential, only for members of the consortium (including the Commission Services)

List of Partners concerned

Partner number	**Partner name**	**Partner short name**	**Country**	**Date enter project**	**Date exit project**
1	Karlsruher Institut für Technologie	KIT	Germany	M1	M36
2	Interuniversitair Micro-Electronica Centrum vzw	IMEC	Belgium	M1	M36
3	Technische Universiteit Eindhoven	TU/e	Netherlands	M1	M36
4	Research And Education Laboratory In Information Technologies	AIT	Greece	M1	M36
5	Universitat de Valencia	UVEG	Spain	M1	M36
6	St Microelectronics	ST	Italy	M1	M36
7	Universiteit Gent	UGent	Belgium	M1	M36

Deliverable Responsible

Organization: Karlsruhe Institute of Technology
Contact Person: Argishti Melikyan
Address: Institute of Photonics and Quantum Electronics
Engesserstr. 5, Building 30.10
76131 Karlsruhe
Germany
Phone: +49 (0)721 – 608 42496
Fax: +49 (0)721 – 608
E-mail: argishti.melikyan@kit.edu

Executive Summary

This document shall incorporate (all) rules procedures concerning the technical and administrative management of the project and is therefore to be updated on a regular basis. Please look at www.navolchi.eu regularly for the latest version.

Change Records

Version	Date	Changes	Author
0.1 (draft)	2012-01-26	Start	Argishti Melikyan
1 (submission)	2012-01-31		-----

Table of Contents:

Background

High speed chip-to-chip interconnects are essential for the realization of latest high-speed computing devices and ultra-compact system-in-a package solutions [1]. They are needed to further leverage products such as computers, mobile phones, HDTV, cameras etc. [2]. High speed I/Os with lowest power consumption can be realized by means of light and optical interconnects, which so far has shown to be capable of encoding up to 26 Tbit/s of data onto a single laser [3]. However, chip-to-chip optical interconnection requires high speed optical transceivers monolithically integrated on electronic ICs, which can convert digital information from electrical domain to optical domain and vice versa. Such transceivers should be compact, offer large bandwidth and consume little power in order to be economically and technologically efficient.

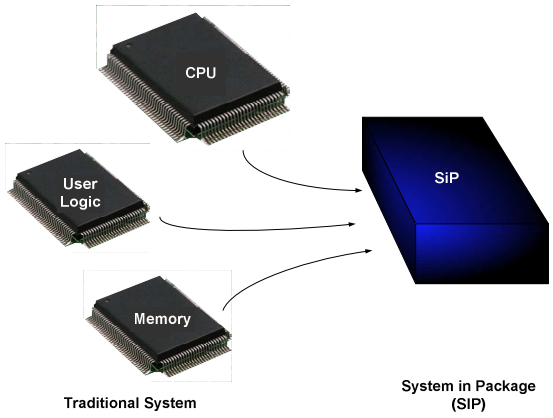

Figure 1 System in a Package (SiP) comprising a CPU, user logic and memory.

The NAVOLCHI project aims in developing of future optical interconnects with high speed, ultra-compact and low power consumption properties. In the NAVOLCHI's interconnection approach, the area devoted to the physical layer of the optical interconnects is reduced by making use of the plasmonic devices which give a possibility to overcome the diffraction limit of the light, thus confining and manipulating light in ultra-compact dimensions.

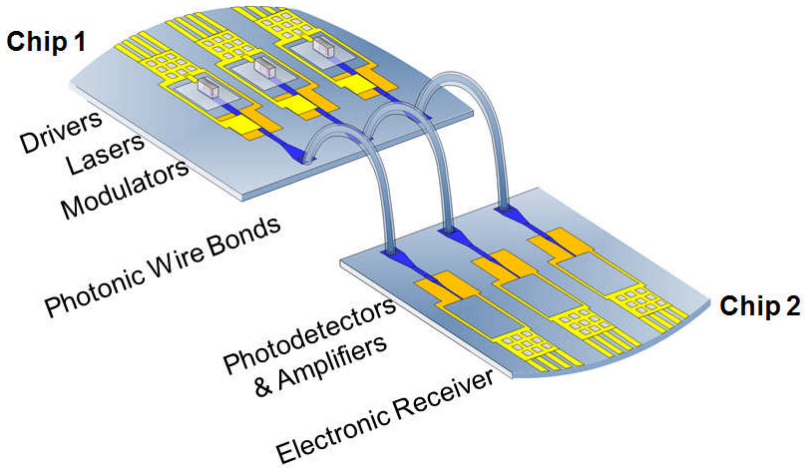

Figure 2 Interconnection of two CMOS chips with plasmonic lasers, photodetectors, fibres, amplifiers and drivers can be seen.

The entire interconnection architecture of the NAVOLCHI is depicted in Figure 2. Infrared light generated in plasmonic nano-lasers bonded on CMOS chip couples to the passive low loss silicon waveguide which serve as a passive link among various plasmonic devices. Light guided through silicon nanowire is coupled to plasmonic modulator where the information is converted from electrical domain to optical domain. After the plasmonic modulator light is coupled out of the chip into the photonic wire bond by means of diffraction gratings. Above described devices all together make one part of the plasmonic physical layer - plasmonic transmitter. Plasmonic receiver consists of the plasmonic photodetectors directly connected to the electronic receiver. Ultra-compact footprints of the plasmonic devices give a possibility of integrating many parallel physical optical links, therefore, increasing the data traffic between two chips.

Two modulator structures have been studied in NAVOLCHI - namely the surface plasmon polariton absorption modulator [4], where the intensity of SPP is directly modulated by plasma effect in metal oxide, and surface plasmon polariton phase modulator [5], where the phase of SPP is modulated making use of the Pockel's effect, see Figure 3.

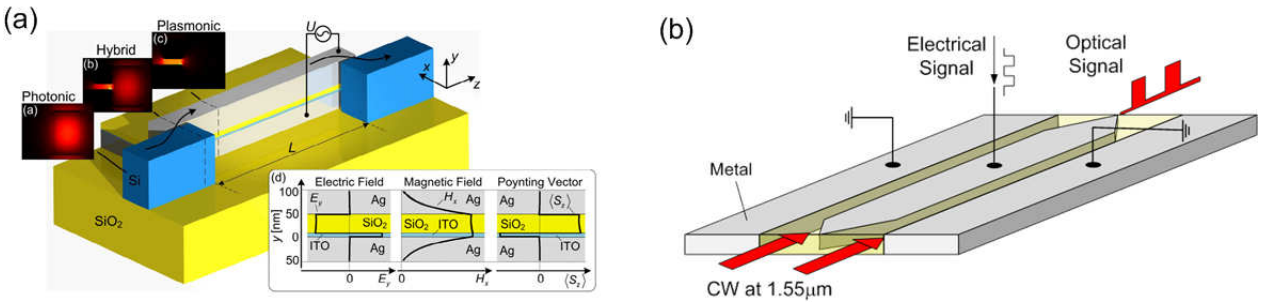

Figure 3 Plasmonic modulator approaches engaged by NAVOLCHI. (a) Surface plasmon polariton absorption modulator [4] and (b) plasmonic phase modulator[5].

Here are the requirements of the plasmonic modulators to be design:

Table 1 The requirements on the plasmonic modulators

Operation wavelength	1.55μm	Insertion loss	< 20dB
Total length	< 50μm	Data rate	7.2Gb/s
Maximum voltage	$4.5V_{pp}$	Latency	<8.8 ns
Silicon compatibility	yes	Electrical energy consumption	~15 pJ/bit

Here, we discuss the theoretical modelling of the plasmonic modulator and its interface with silicon photonics. Particularly, we describe the semi - numerical and numerical methods used for optimization and estimation of the figure of merits for various modulator structures. Important characteristics, such as modulation index, footprint, driving voltage, optimum operation wavelength range, bandwidth, insertion loss as well as its integration with silicon photonics, are discussed.

1. General Modelling

Below we briefly describe semi numerical models which have been developed for quick estimation of the performance of the plasmonic devices without running power and time hungry complicated full vectorial numerical simulations such as FDTD or FEM. First we describe the derivation of the dispersion relation of arbitrary number of multilayer structure and then we show how the Poisson equation is solved numerically for the surface plasmon polariton absorption modulator.

1.1 Dispersion Relation for Multilayer Slab Structure

In order to study various configurations of plasmonic devices we developed a numerical model which calculates the dispersion relation of SPP at arbitrary multilayer slab structure. The model is implemented in Matlab and is similar to the one reported in [6]. Assuming N dielectric layers are stacked along the *x*-directions and are homogenous along *y* and *z* axis, we can employ Maxwell's equation to derive the scalar wave equation in each layer for the transverse magnetic (TM) polarized light

$$\frac{\partial^2 H_y^n(x)}{\partial x^2} + (k_0{}^2 \varepsilon_n - \beta^2) H_y^n(x) = 0 \tag{1}$$

where we have assumed the $\mathbf{H}(r,t) = \mathbf{H}(x,y)e^{i(\omega t - \beta z)}$ time and *z* dependence of monochromatic light, where β is the wave vector along the propagation direction i.e. the propagation constant, ε_n is the dielectric permittivity of the *n*th layer, $k_0 = \omega/c$ is the wave vector of light in vacuum. Additionally, we have used the fact that for the TM eigenmodes of interest it holds that $H_x^n = 0, H_z^n = 0$ as well as $\partial H_y^n(x,y)/\partial y = 0$.

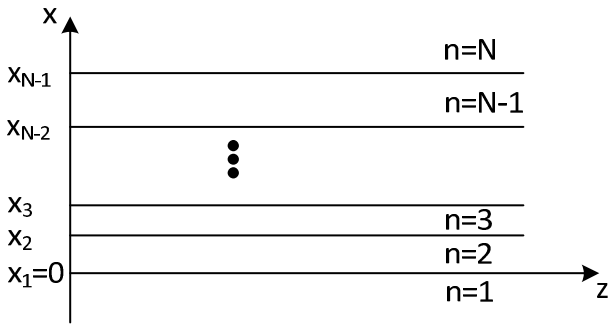

Figure 4 Geometrical structure of the multilayer slab waveguide. Layer n=1 and n=N extend to minus and plus infinity, respectively. Layers n=2...N-1 have certain thicknesses of x_n - x_{n-1}.

The solution of the scalar wave equation (1) in each layer can be given in the form

$$H_y^n(x) = H_y^{n+} e^{-jk_x^n(x - x_{n-1})} + H_y^{n-} e^{jk_x^n(x - x_{n-1})} \tag{2}$$

where k_x^n is the wave vector along the *x*-axis, H_y^{n+} and H_y^{n-} are amplitude magnetic field of the waves propagating along positive and negative directions of *x*-axis respectively. Substituting the Ansatz (2) into the scalar wave equation (1) transverse component of wave vector can be given as $k_x^n = \sqrt{k_0^2 \varepsilon_n - \beta^2}$. In addition the amplitudes of the magnetic field in each layer is connected

to the amplitudes of in the neighbouring layers by means of boundary conditions for electric and magnetic fields at the interfaces, which results to [6]

$$\begin{bmatrix} H_y^{n+1} \\ H_y^{n+1} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 & \varepsilon_{n+1}/k_{n+1} \\ 1 & -\varepsilon_{n+1}/k_{n+1} \end{bmatrix}\begin{bmatrix} 1 & 1 \\ k_n/\varepsilon_n & -k_n/\varepsilon_n \end{bmatrix} \times \begin{bmatrix} \exp(-jk_n(x_n - x_{n-1})) & 0 \\ 0 & \exp(jk_n(x_n - x_{n-1})) \end{bmatrix}\begin{bmatrix} H_y^{n+} \\ H_y^{n+} \end{bmatrix} \tag{3}$$

As a result the magnetic field amplitudes in Nth layer can be expressed by the amplitudes of the field in n=1 layer.

$$\begin{bmatrix} H_y^{N+} \\ H_y^{N-} \end{bmatrix} = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix}\begin{bmatrix} H_y^{1+} \\ H_y^{1-} \end{bmatrix} \tag{4}$$

Guided modes are characterized by the property that there is no light falling onto the structure from plus and minus infinity i.e. $H_y^{1+} = 0$ and $H_y^{N-} = 0$. These equalities fulfill only when $M_{22} = 0$. The set of β and ω in which cases the latter equality fulfills define the dispersion relation of the eigenmodes in the structure. The dispersion relation is found by numerically finding the set of β for the given ω in which case M_{22}=0. Typical dispersion relation of the metal-insulator-metal structure is given in Figure 6 by means of real and imaginary parts of the propagation constant β.

1.2 Thomas Fermi Screening

When conductive materials such as highly doped semiconductors or metal films are brought under the static electric field the charge accumulation layer is formed at the interface of the conductor because of the well-known screening effect. Controlling such a charge density at the metal interface by the applied electric field has been previously used for the modulation of surface plasmon polaritons [4,7-8]. For a proper estimation of this effect we employ the Thomas-Fermi screening method described in [4]. Having found already the free carrier density at the accumulation layer, the complex dielectric permittivity of the conductor which is under the external electric field can be modelled via the Drude model.

The Poisson equation relates the electric potential $\phi(y)$ to the induced charge density $N_{\mathrm{i}}(y)$ within the conductor layer

$$\Delta\phi(y) = \frac{e(N_{\mathrm{i}}(y) - N_0)}{\varepsilon_0\varepsilon_{\mathrm{r}}} \tag{5}$$

Here, e is the elementary charge, ε_0 is the vacuum permittivity, ε_{r} is the relative static permittivity of the conductor, and N_0 is the bulk free carrier density of the conductor. Following the Thomas-Fermi approach the total free carrier density and the potential are related by

$$N_{\mathrm{i}}(y) = \frac{1}{3\pi^2}\left(\frac{8\pi^2 m_{\mathrm{eff}}}{h^2}\right)^{3/2}\left(E_F + e\phi(y)\right)^{3/2} \tag{6}$$

where the Fermi energy is defined as

$$E_F = \left(\frac{h^2}{8\pi^2 m_{\text{eff}}} \left[3\pi^2 N_0 \right]^{2/3} \right) \tag{7}$$

In the latter expression h is Planck´s constant and m_{eff} the electron effective mass. We numerically solve Eq. (5) with Eq. (6) – (7) for the conductor interface using mixed boundary conditions, that is, for the given gradient of electric potential outside of the conductor and zero electric potential inside the conductor far away from the interface.

2. Plasmonic Modulator Approaches

Here we discuss two modulator approaches, namely, direct amplitude modulation employing surface plasmon polariton absorption modulator [4,7] and phase modulation with plasmonic phase modulator [5].

2.1 Surface plasmon polariton absorption modulator

Surface plasmon polariton absorption modulator is a device where the absorption coefficient of surface plasmon polariton (SPP) is modulated by an externally applied voltage. The essential parts of the SPPAM are highly conductive metal layers (e.g. Au, Ag) and middle active section consisting of metal oxide (Indium Tin Oxide) and high dielectric strength insulator (SiO_2, HfO) layers, see Figure 5. Such a structure sustains highly confined SPP mode, which represents strong optical field confinement in ultrathin metal oxide layer [4, 7]. Consequently, the dispersion relation of the SPP is predominantly sensitive towards the optical properties of ITO thin film, particularly to its free carrier density. The voltage applied between the two electrodes induces charge accumulation layer in ITO as depicted in Figure 5(c). As a result, the free electron density of ITO is modified by the applied voltage which results in a change of the absorption coefficient of SPP.

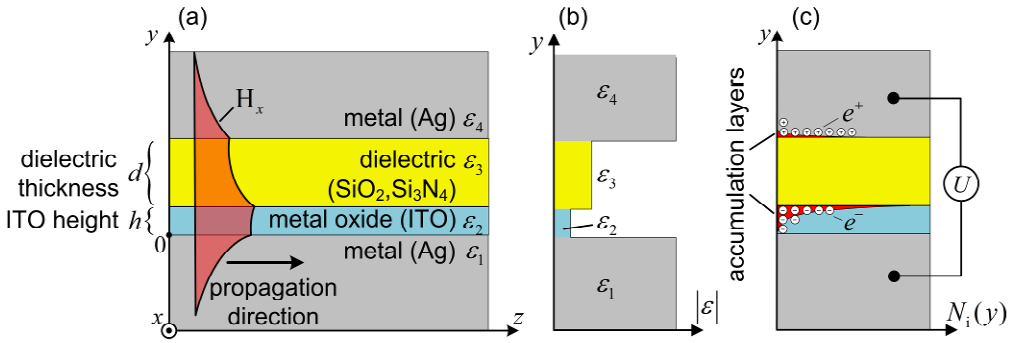

Figure 5 Plasmonic structure with metal/dielectric/metal-oxide/metal layers. (a) Geometry and (b) dielectric permittivity distribution. The H_x component of the SPP magnetic field is schematically shown as a contour filled with reddish colour in (a). The SPP propagates along the positive *z*-direction. (c) Carrier density distributions $N_i(y)$ in both electrodes [4].

Typical dispersion relation of SPP at the SPPAM obtained from the above described method is given in Figure 6. For the sake of this example the propagation constant and SPP absorption coefficients for the Ag/ITO(8nm)/Si_3N_4(70nm)/Ag structure are given for two different free carrier densities of ITO. It can be seen that slight change of the free carrier density of ITO results in significant modulation of SPP absorption coefficient.

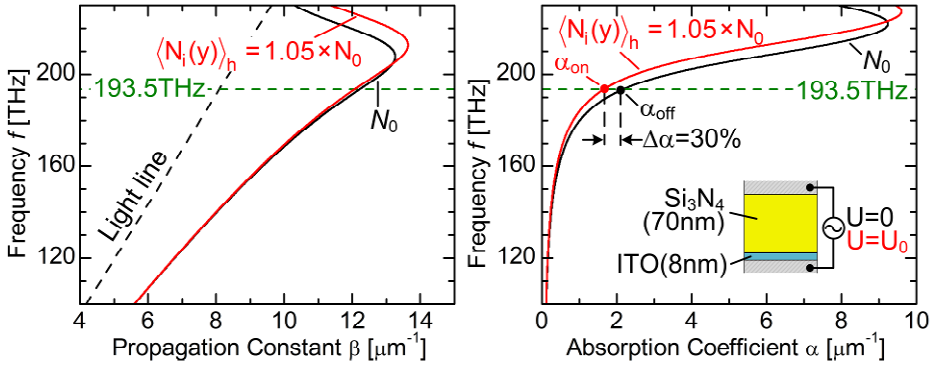

Figure 6 Dispersion relation of SPP guided by the Ag / ITO(8nm) / Si_3N_4(70nm) / Ag layer stack. Both, propagation constant and absorption coefficient change when the carrier density of ITO is increased by 5 % (red lines). As opposed to the propagation constant the absorption coefficient varies significantly with ITO carrier density.

To estimate the performance of the various configurations of the SPPAMs we have used the combination of the dispersion relation (Section 1.1.) and the accumulation layer (Section 1.2) solvers. In Figure 7, we give the structures which have been considered as possible candidates for the SPPAM.

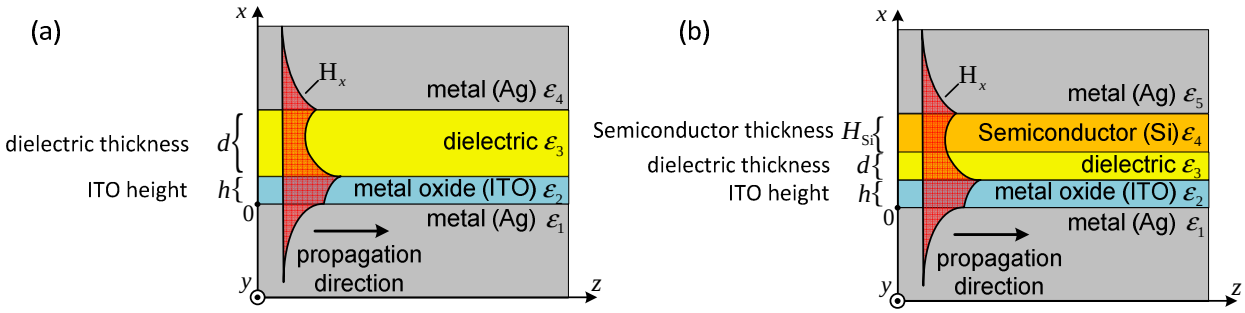

Figure 7 The SPPAM geometrical structure studied in NAVOLCHI. The SPPAM approach reported comprising metal / metal-oxide / dielectric / metal layers (a) and metal / semiconductor / metal-oxide / dielectric / metal layers (b), respectively.

Structure depicted in Figure 7(a) is the conventional SPPAM comprising two silver electrodes, high dielectric strength insulator (SiO_2, HfO) and Indium Tin Oxide as an active layer [4]. The structure has the advantages that it is potentially free from carrier-related speed limitations. Moreover, the entire voltage drop is mainly across the insulator layer which increases the electron density in the accumulation layer formed in the metal oxide layer. However, it is very challenging to excite the SPPs in structures with relatively small insulator thicknesses *d*.

Structure depicted in Figure 7(b) is similar to the one reported in [7], however, with second silver electrode brought into contact with semiconductor. The voltage drop in this structure is across the semiconductor and insulator resulting in the reduced accumulation layer at ITO interface for the given *d* (comparing to the first approach). However, because a semiconductor based SPPAM can be fabricated with ultrathin insulator thicknesses, the accumulation layer can still be enhanced comparing to the first approach [7]. Moreover, it has been demonstrated previously that the SPP at such a structure can efficiently be excited using the conventional silicon nanowire photonic mode [7].

Here we compare the semiconductor based structure, see Figure 7(b), with the metal based structure reported previously, see Figure 7(a) [4]. We again define figure of merit of the structure

$$\mathrm{FoM} = \frac{L_e}{L_{1\mathrm{dB}}} \tag{8}$$

where the L_e is the propagation length of SPP and $L_{1\mathrm{dB}}$ is the length necessary for having an extinction ratio of 1dB for the given $4.5\mathrm{V_{pp}}$ voltage. The larger the FoM, the better the performance of the modulator is, i.e. the lower the propagation losses are for a 1 dB extinction ratio and an applied on-voltage of 4.5 $\mathrm{V_{pp}}$. Overall the report the silicon thickness H_{Si} is assumed to be 220nm.

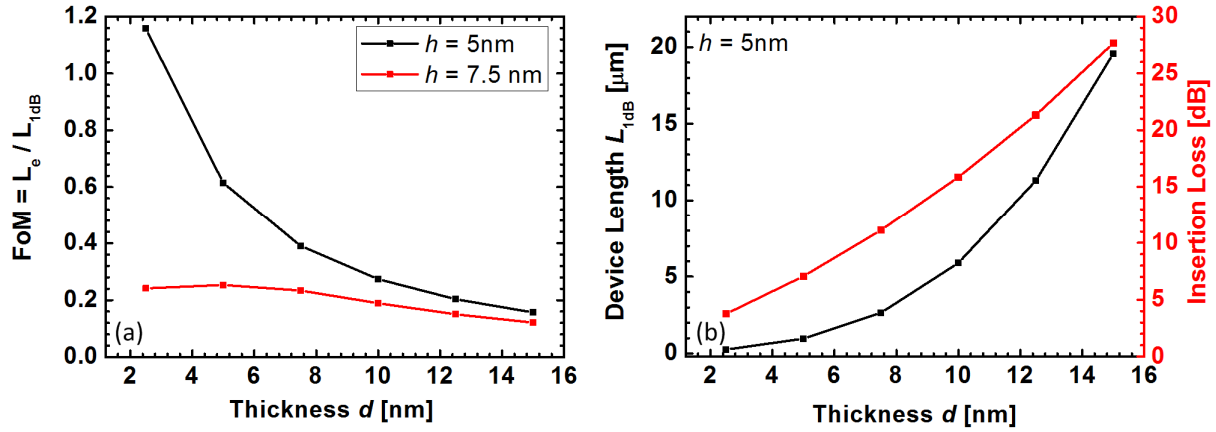

Figure 8 Characteristic quantities of semiconductor based SPPAM. The figure of merit for various silicon dioxide and ITO thicknesses (a) and 1dB device length and insertion loss for 5nm of ITO thickness

It has been found that the figure of merit for the semiconductor based SPPAM is significantly larger than the one of the pure metal based SPPAM reported in [4]. As a result, in Figure 7(b) we give the device length $\mathrm{L_{1dB}}$ providing 1dB extinction ratio for the $4.5\mathrm{V_{pp}}$ applied voltage as well as the insertion loss of the device. It can be seen that micrometer scale device can be designed with relatively low insertion loss making use of the semiconductor based SPPAM approach.

Hafnium oxide (HfO) which is well known insulator material in semiconductor industry has also been considered as alternative to silicon dioxide.

2.2 Surface plasmon polariton phase modulator

SPP based phase modulator can be designed making use of metal-insulator-metal structure and replacing passive insulator layer with linear electro-optically active nonlinear optical (NLO) material. Externally applied static electric field E_{stat} changes the refractive index of the NLO material, thus changing the phase of the SPP mode, see Figure 9. The refractive index change happening in the nonlinear material can be given as [9]

$$\Delta n = \frac{1}{2} r_{33} n_{\mathrm{NLO}}^3 E_{\mathrm{stat}} = \frac{1}{2} r_{33} n_{\mathrm{NLO}}^3 \frac{U}{d} \tag{9}$$

where r_{33} and n_{NLO} are the linear electro-optic coefficient and the refractive index of the nonlinear material, E_{stat} is the strength of the static electric field. Typical NLO materials studied in NAVOLCHI are electro-optic polymers with a typical refractive index n_{NLO} of 1.6 and 1.7. Such NLO material can be synthesised with relatively large nonlinear coefficient thus ensuring the ultra-compact size of the device as well as small driving voltage [10].

Material	Refractive index n_{NLO}	Linear electro-optic coefficient r_{33}
Polymer 1 [10]	1.7	70pm/V
Polymer 2 [11]	1.6	70pm/V

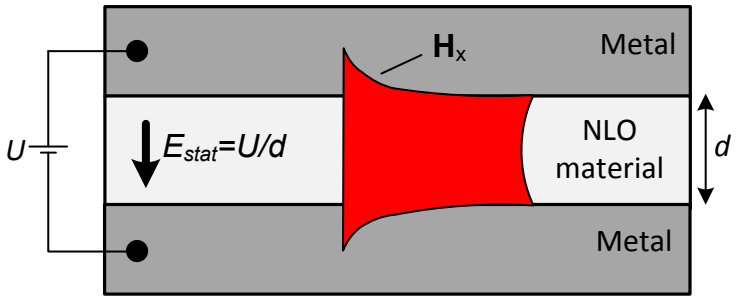

Figure 9 Geometry of the plasmonic phase modulating comprising linear electro-optically active material sandwiched between two metals

Dispersion relations of the even SPP mode at metal (Ag) – polymer (n_{NLO} = 1.6) – metal (Ag) structure is depicted in Figure 5. For the sake of this example, the thickness of the polymer layer is assumed to be d = 30nm. The normal component of the electric field and the transverse component of the magnetic field of the fundamental even SPP mode are given as insets in the Figure 10. It can be seen that the most of the field is confined inside the active region of the device. This ensures light - nonlinear polymer strong interaction. The change occurring in both real and imaginary parts of the propagation constant β can be seen when $U = 4.5V_{pp}$ voltage is applied on the structure. The significant change occurs in relatively high frequency range which is a result of low group velocities of SPP in that frequency range. However, because of the limitation on the plasmonic laser operation wavelength, the plasmonic phase modulator is designed for the operation in 193.5THz frequency which corresponds to the 1.55μm wavelength, where the plasmonic laser is proved to operate well and silicon is well transparent.

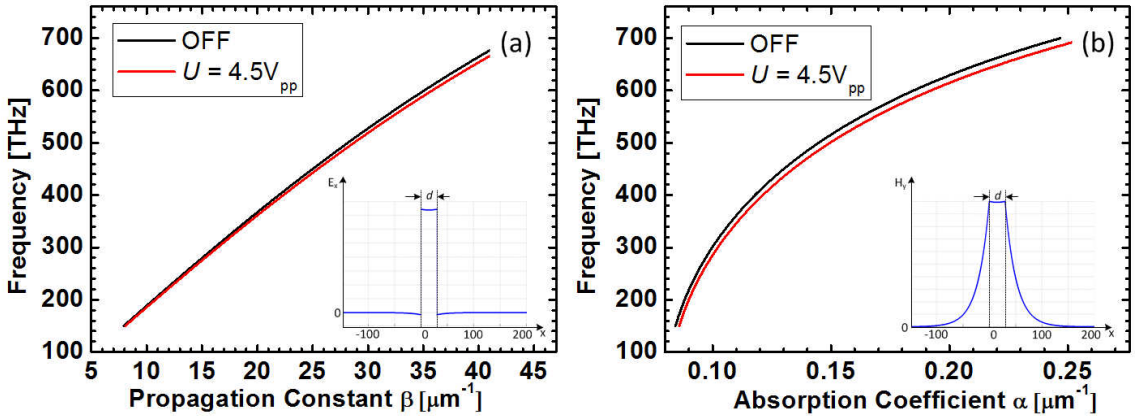

Figure 10 (a) The propagation constant $\mathrm{Re}(\beta)$ and the absorption coefficient $2\,\mathrm{Im}(\beta)$ for the silver – polymer - silver structure in Off and On (U = 4.5 V_{pp}) cases and for the d = 30nm. The normal component of the electrical field and the transverse component of magnetic field profiles in the structure are given as insets in (a) and (b), respectively.

In order to compare various structures we define the figure of merit as a ratio of the SPP propagation length L_e over the length L_π necessary for accumulating a phase shift of π relative to the voltage off state:

$$\mathrm{FoM} = \frac{L_e}{L_\pi} \tag{10}$$

the larger FoM, the shorter L_π and the longer L_e are i.e. the smaller the device footprint and the insertion losses are.

The first decision that has to be made on the modulator structure is the material system which has to be used, that is the choice on the metal electrodes as well as on the nonlinear polymer. We have assumed commercially available NLO polymer [10] with a refractive index of 1.6 and 1.7. The high conductivity of the metal electrodes ensures the potentially high speed characteristics of the device. Therefore, the choice of the metal only depends on technological aspects as well as on their optical losses. It is well known that silver has the highest conductivity and thus the least optical losses, consequently, the structure employing silver electrodes result in a higher figure of merits, see Figure 11. Increasing the refractive index of the insulator – in this case of the polymer - the characteristic surface plasmon frequency reducing resulting in lower group velocity, thus resulting in reduction of the L_π via enhancement of light-matter interaction.

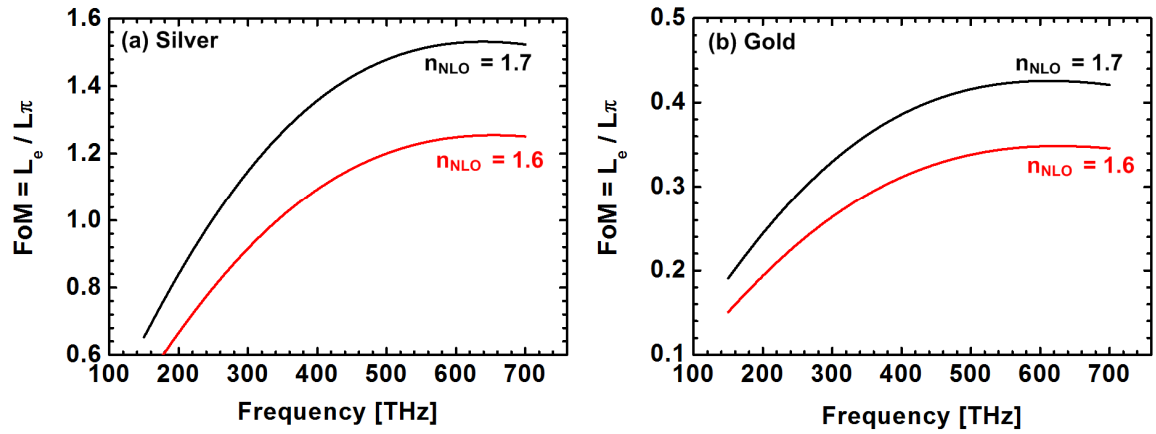

Figure 11 The comparison of the FoMs of the metal - polymer - metal structure for various metals and nonlinear polymer refractive indices. The polymer height *d* has assumed to be 30nm. Applied voltage across the device is U = 4.5V$_{pp}$

Even though the silver electrodes provide much larger figure of merit, gold is considered to be still good electrodes for the plasmonic phase modulator because of its very important advantages such as no oxidation, stable properties as well as good quality of the deposited layers.

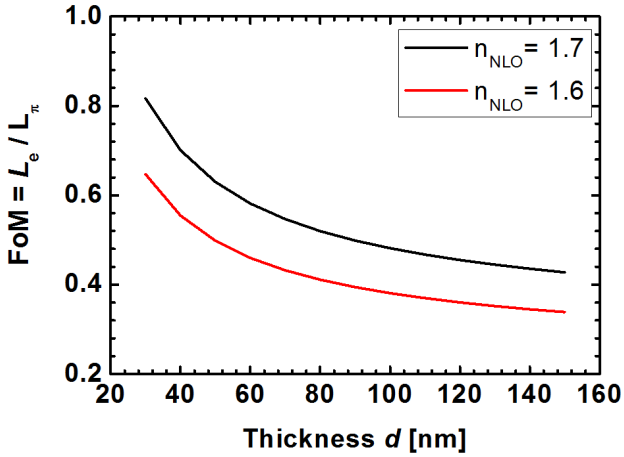

Figure 12 Figure of merits of the device for various nonlinear material size *d* and for n_{NLO} = 1.6 and n_{NLO} = 1.7 refractive indices. In the calculation applied voltage is assumed to be 4.5 V_{pp}. Silver electrodes has been considered.

Another important property in modulator design is the active area size *d* height. For the sake of the above examples, it has been assumed that the polymer height is 30nm. However, fabrication of such thin films as well as excitation of the SPP in such a dimensions are rather challenging, therefore, the possibility of the larger active area size should be considered. Below, we show the figure of merit calculated for the various polymer heights for the case of both silver and gold.

In summary, we can conclude that the performance of the device strongly depends on the polymer thickness *d* especially in the range of the small values and saturates while increasing the thickness *d*. Because of the technological challenges in fabrication process, the polymer thickness below 50nm are ignored and the focus has been paid more on the relatively large polymer thickness i.e. above 50nm.

Below we show the overall device length and the total insertion loss (not including the coupling losses) for various polymer thicknesses *d*. The polymer is assumed to have refractive index of 1.7 and linear electro optic coefficient of 70pm / V.

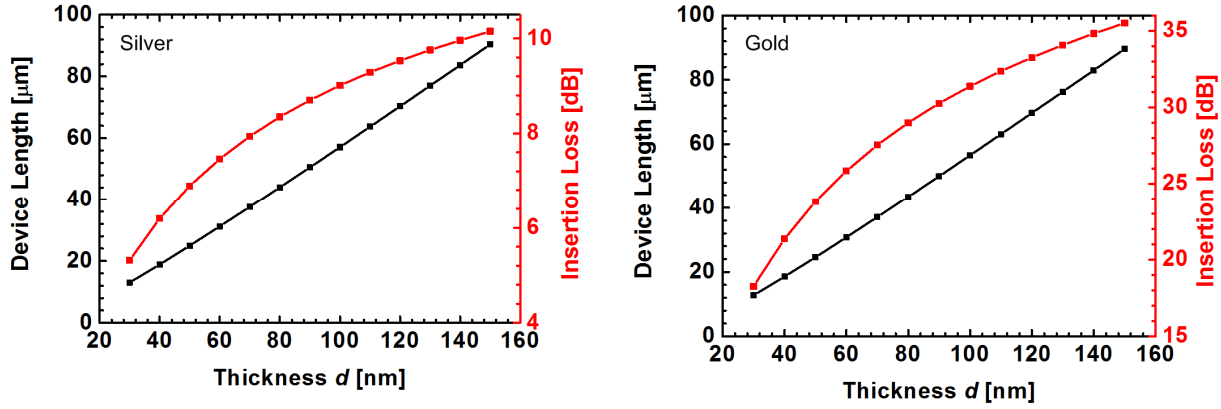

Figure 13 Device length and the insertion loss for the operating voltage of 4.5V_{pp}. Polymer is assumed to have a refractive index of 1.7 and nonlinear coefficient of 70pm/V. The electrodes have been assumed to be (a) silver and (b) gold.

3. Decision on Plasmonic Modulator

Two decisions have been made concerning to the plasmonic modulator:

1. The plasmonic phase modulator approach is preferred over the SPPAM reported in [4] and given in Figure 14, because of its relatively large figure of merit and easy coupling structure. The decision is also supported by the fact that the plasmonic phase modulator is relatively easier to fabricate comparing to the absorption modulator [4]. Below we give the possible approach for fabricating plasmonic phase modulator.

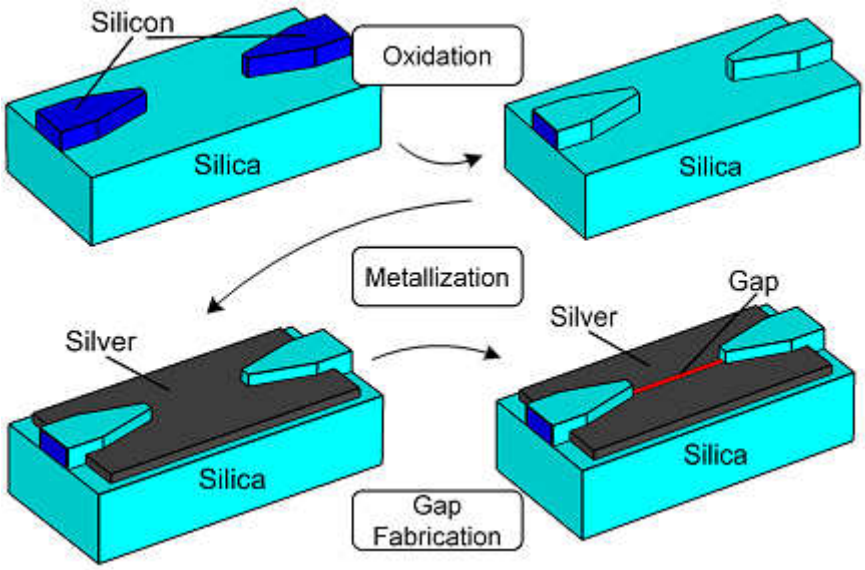

Figure 14 Process flow for fabrication of the plasmonic phase modulator

2. Additional efforts will be spent on optimization of the semiconductor based 3D real SPPAM and its coupling to silicon nanowire waveguide.

4. 3D Phase Modulator Design

Here, we discuss vertical slot type structure where two metal sheets are brought close to each other forming nanoscale gap in between, forming so called plasmonic vertical slot waveguide, see Figure 15. Such a plasmonic vertical slot waveguide is the 3D equivalent of the device depicted in Figure 9. Such a structure sustain a SPP mode confined not only horizontally across the slot, but also vertically. Typical mode profile in the structure is given in Figure 15. In addition to above calculations, we cross checked the results obtained for 2D slab structure by making full vectorial FEM mode analyses with COMSOL Multyphysics.

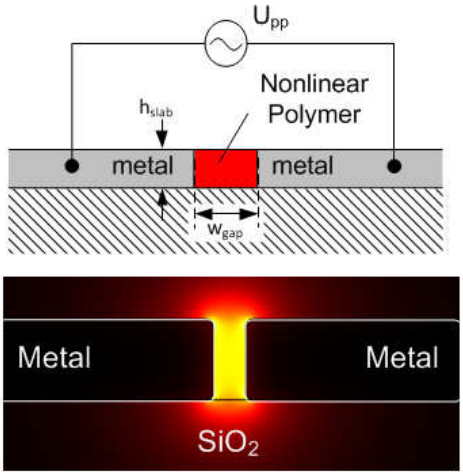

Figure 15 Real 3D plasmonic phase modulator and the optical mode confined in the polymer slot.

The figure of merit as well as the latency for real 3D device are given below for the polymer refractive index of 1.7 and for various plasmonic slot width w_{gap} and metal thickness of h_{slab}.

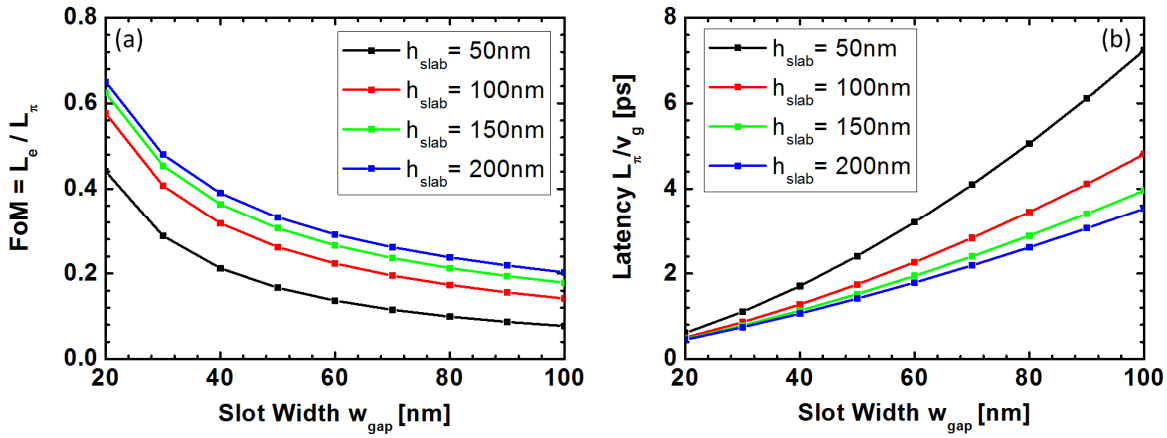

Figure 16 Figure of merit of the real 3D modulator (a) and the latency of the device with a length of L_π (b). The polymer with a refractive index of 1.7 and the applied voltage of 4.5Vpp are taken.

For the real 3D modulator, smaller figure of merits have been found comparing to the slab type. The reason is the reduction in the optical field confinement inside active region, while reducing the thickness of the metal electrodes. The latter also can be seen in Figure 16(a). Latency has been calculated as the time that the pulse with a central wavelength of 1.55μm takes to travel through the length L_π.

It can be seen from Figure 16, that the modulator provides its best performance for the metal thicknesses larger than 100nm and for the slot size below 80nm. The possibility of the slot size smaller than 50nm is being omitted because of the fabrication limitation.

5. Photonic – Plasmonic Interface Development

Efficient couplers are necessary which will provide good coupling between the low loss silicon nanowire waveguide and the plasmonic vertical slot waveguide, see Figure 17. Moreover, from the above calculations it can be seen that the figure of merit of the phase modulator increases with reducing the size of the plasmonic slot. Such aggressive downscaling of the plasmonic slot makes the SPP excitation even more challenging because of the strong dimension mismatch between silicon nanowire and plasmonic slot waveguides.

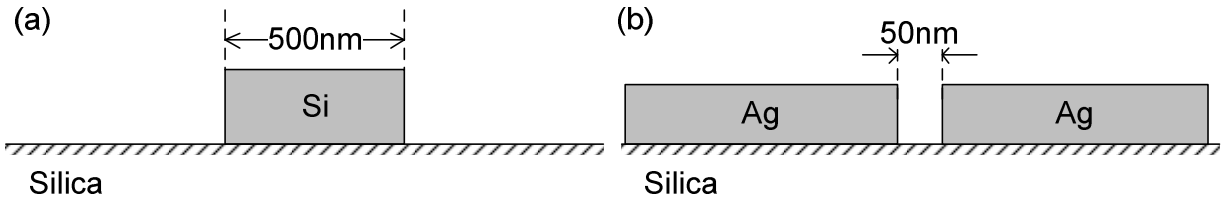

Figure 17 Typical waveguides used in (a) silicon photonics and (b) in active plasmonics.

5.1 Tapered Couplers

The most promising approach to couple light from a silicon nanowire to a plasmonic slot waveguide is the tapered metallic coupling configuration which provides very large and broadband coupling efficiency [12]. In such a coupling scheme, quasi-TE polarized light guided through silicon nanowire is adiabatically squeezed and launched into the plasmonic slot waveguide, see Figure 18(a).

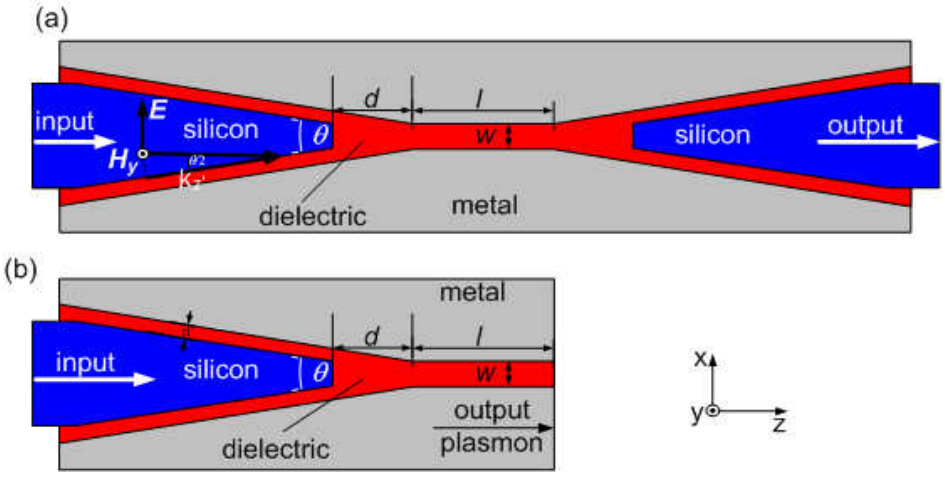

Figure 18 Geometry of plasmonic coupler, (a) top view of the realistic plasmonic modulator with two coupling sections and (b) structure used in optimization

The coupler is optimized for its highest transmission for the given silicon width of 500nm, dielectric material with a refractive index of 1.6 and 1.7. The realistic plasmonic modulator consists of two coupling sections for in- and out-coupling of the active region with a length of *l* as it is depicted in Figure 18(a). However, because of the limitation of the computational power,

we have restricted ourselves in optimizing a single coupling section as the structure is symmetric relative to the central active section.

5.1.1 Methods and Results

To calculate the SPP excitation efficiency we have performed simulation of the propagation of electromagnetic wave based on the Finite Integration Technique (CST Microwave Studio). To avoid from additional complexities in the computational, first the simulations have be carried out for 2D structure i.e. no refractive index variation along *y*-axis. The excitation efficiency of SPP in the metal-dielectric-metal structure is calculated as normalized transmission coefficient from the silicon waveguide to the plasmonic waveguide

$$transmission = \frac{P_{out}}{P_{in}} \tag{11}$$

where the P_{in} is the power at the input of the silicon waveguide and P_{out} the power at the output of the plasmonic waveguide, see Figure 18(b). The *transmission* is calculated varying the angle of the silicon tip θ, separation of plasmonic and silicon waveguides d. This is done for various plasmonic slot widths and dielectric refractive indices. The results of the refractive index of 1.6 are summarized in Figure 19.

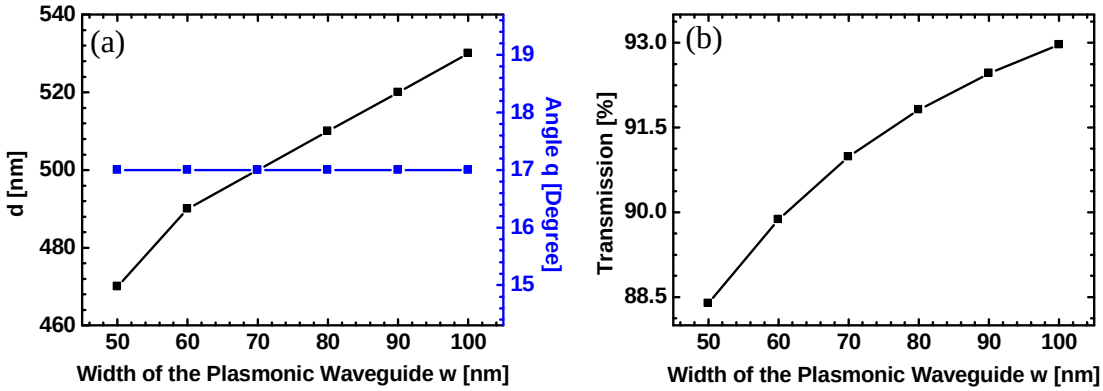

Figure 19 The optimized couplers geometry for various plasmonic waveguide widths *w*. (a) Optimized silicon tip angle θ and distance *d*. (b) Transmission corresponding to optimized structure

It can be seen that the coupler provides the maximum coupling efficiency for the certain silicon tip angle of 17 degrees. Slight dependence of the optimum distance *d* on plasmonic waveguide width *w* can be seen. In all the cases the normalized transmission exceeds 85%, see Figure 19(b), which makes such approach of SPP excitation unique.

The results have been confirmed for 3D realistic coupler with the metal and silicon heights of 220nm. In Figure 20 we show the typical field propagation in the coupler in the terms of magnetic H_y and electric E_y fields.

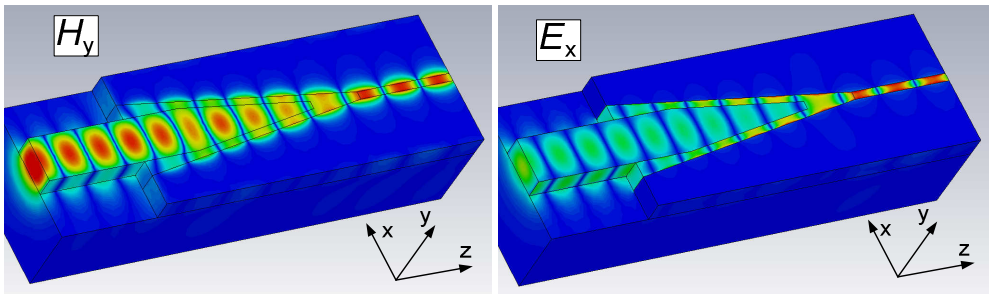

Figure 20 H_y and E_x component of the electromagnetic wave propagating through the plasmonic coupler (3D).

An example of the geometrical parameters of the 3D realistic coupler can be found in Table 2.

Table 2 The geometrical parameters of the coupler for 50nm plasmonic slot width

SOI device layer thickness	220nm
Silicon waveguide width	500nm
Plasmonic slot width	>50nm
Distance *d*	75nm
Angle θ	15°-17° (36° for 50nm slot size)
Efficiency of a single coupler	87%

6. Electrical Modelling Plasmonic Phase Modulator

Plasmonic phase modulator is a device based on linear electro optic Pockel's effect which is an instantaneous effect. Therefore, the possible speed limitations can only origin from electronic properties of the device. Below we discuss this issue.

Because of its short length, the plasmonic phase modulator can be modelled as a lumped element with a capacitor and a resistor connected in parallel, see Figure 21, where the capacitor describes the charge accumulation at the metal interfaces and the resistor describes the leakage current. The nonlinear optical polymers, such the ones discussed above, in our experiments introduce very small leakage current, in the range of 20nA. Therefore, we can neglect the parallel connected resistance and assume that the device is a capacitor connected to the voltage generator with a 50Ω internal impedance. As a result we end up with a low pass characteristic circuit with a cut off frequency of 1THz.

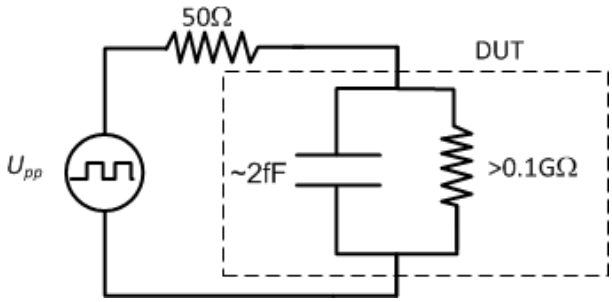

Figure 21 Lumped element model of the plasmonic phase modulator.

7. Conclusion & Outlook

As a result of overall modelling the following modulator characteristics are obtained:

Operation wavelength	1.55μm	☺	Insertion loss	< 20dB	😐
Total length	< 50μm	☺	Data Rate	>50Gb/s	☺
Maximum voltage	$4.5V_{pp}$	☺	Latency	<3 ps	☺
Silicon compatibility	yes	☺	Electrical energy consumption	~15 pJ/bit	😐

Almost all the required specification on the modulator can be fulfilled employing plasmonic phase modulator. It is relatively more challenging to reduce the optical losses in the system.

We are currently carrying out fabrication and characterization of the plasmonic couplers and modulators fabricated on SOI chips provided by IMEC. In figure 22, we show an SEM image of the complete plasmonic phase modulator comprising two taper couplers and metallic nanoslot in between.

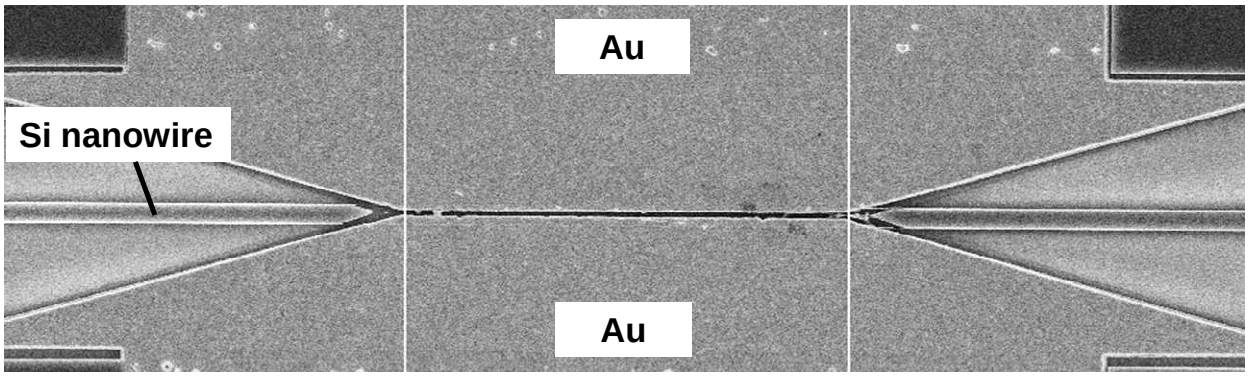

Figure 22 Scanning electron microscope image of the plasmonic phase modulator.

References

[1] I. A. Young, *et al.*: Optical I/O Technology for Tera-Scale Computing, *IEEE J. of Solid State Circuits*,
vol. 45. pp. 235-248, Jan. 2010.
[2] System-in-Package: The New Wave in 3D Packaging, TechSearch International, Inc., September 2005.
[3] D. Hillerkuss, *et al.*: 26 Tbit s−1 line-rate super-channel transmission utilizing all-optical fast Fourier transform processing, *Nat. Photon*ics, vol. 5, pp. 364–371, May 2011.
[4] A Melikyan, N. Lindenmann, S. Walheim, P. M. Leufke, S. Ulrich, J. Ye, P. Vincze, H. Hahn, T. Schimmel, C. Koos, W. Freude, and J. Leuthold, "Surface plasmon polariton absorption modulator.," *Optics express*, vol. 19, no. 9, pp. 8855–69, Apr. 2011.
[5] S.-I. Inoue and S. Yokoyama, "Numerical simulation of ultra-compact electro-optic modulator based on nanoscale plasmon metal gap waveguides," Electronics Letters, vol. 45, no. 21, p. 1087, 2009.
[6] T. J. Davis, "Surface plasmon modes in multi-layer thin-films," Optics Communications, vol. 282, no. 1, pp. 135–140, Jan. 2009.
[7] E. Feigenbaum, K. Diest, and H. a Atwater, "Unity-order index change in transparent conducting oxides at visible frequencies.," Nano letters, vol. 10, no. 6, pp. 2111–6, Jun. 2010.
[8] R. Ma and X. Zhang, "Ultra-compact silicon nanophotonic modulator with broadband response," vol. 1, pp. 17–22, 2012.
[9] Robert W. Boyd, "Nonlinear Optics" (Academic, 2008), Third Edition
[10] "GigOptix", retrieved http://www.gigoptix.com/.
[11] J. Brosi, C. Koos, L. C. Andreani, J. Leuthold, and W. Freude, "High-speed low-voltage electro-optic modulator with a polymer-infiltrated silicon photonic crystal waveguide" vol. 16, no. 6, pp. 180–185, 2008.
[12] S. Zhu, T. Y. Liow, G. Q. Lo, and D. L. Kwong, "Silicon-based horizontal nanoplasmonic slot waveguides for on-chip integration.," Optics express, vol. 19, no. 9, pp. 8888–902, Apr. 2011.