Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

D 3.3 – Fabrication of plasmonic laser device

Deliverable no.: D3.3
Due date: 01/10/2013
Actual Submission date: 13/04/2015
Authors: TUE
Work package(s): WP3
Distribution level: RE[1] (NAVOLCHI Consortium)
Nature: document, available online in the restricted area of the NAVOLCHI webpage

List of Partners concerned

Partner number	Partner name	Partner short name	Country	Date enter project	Date exit project
1	Karlsruher Institut für Technologie	KIT	Germany	M1	M36
2	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMEC	Belgium	M1	M36
3	TECHNISCHE UNIVERSITEIT EINDHOVEN	TU/e	Netherlands	M1	M36
4	RESEARCH AND EDUCATION LABORATORY IN INFORMATION TECHNOLOGIES	AIT	Greece	M1	M36
5	UNIVERSITAT DE VALENCIA	UVEG	Spain	M1	M36
6	STMICROELECTRONICS SRL	ST	Italy	M1	M36
7	UNIVERSITEIT GENT	UGent	Belgium	M1	M36

[1] **PU** = Public
PP = Restricted to other programme participants (including the Commission Services)
RE = Restricted to a group specified by the consortium (including the Commission Services)
CO = Confidential, only for members of the consortium (including the Commission Services)

Deliverable Responsible

Organization: Eindhoven University of Technology
Contact Person: Victor Dolores-Calzadilla
Address: Faculty of Electrical Engineering
P.O. Box 513
5600 MB Eindhoven
The Netherlands
Phone: +31 (0) 40247 5129
E-mail: v.calzadilla@tue.nl

Executive Summary

The fabrication technology to fabricate the nanolaser device is described in this report. Specialized technology has been developed at TU/e towards the experimental demonstration of such a laser source. A complete process flow for the fabrication of the device which involves eight lithographic steps, was verified. The process is functional and robust, and was used to demonstrate nanoLED devices. Due to internal cavity losses higher than expected, laser operation has not been reached yet. The technology here described is relevant also for other metal-based nanophotonic circuits.

Change Records

Version	Date	Changes	Author
1	2014-02-07	First submission	V. Calzadilla, M. Smit
2	2015-03-10	Updated version	V. Calzadilla, M. Smit

1. Introduction

It is the aim of TU/e within WP3 to develop a nanolaser with a metallic cavity. This report describes the technology development and fabrication process followed to fabricate the waveguide-coupled nanocavities reported in Milestone 40. The III-V samples are adhesively bonded to silicon with BCB (Benzocyclobutene) and processed in the Nanolab Cleanroom at TU/e. A variety of techniques are used including electron-beam lithography, dry and wet etching, as well as deposition of dielectrics and metals.

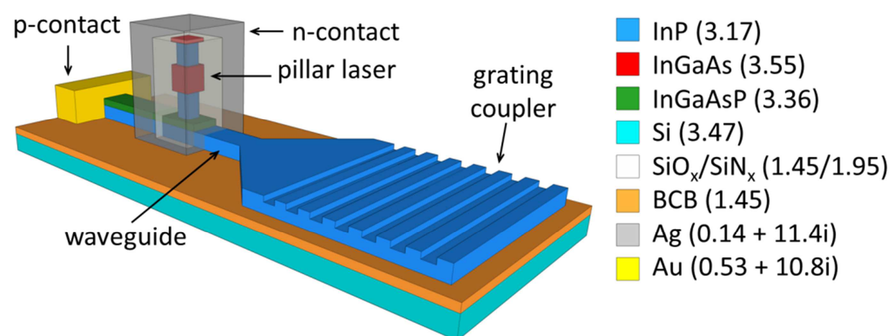


Figure 1. Schematic of the metal-cavity nanolaser that is described in the present fabrication technology report. The refractive index of each material at 1.55 μm is shown in parenthesis.

Figure 1 shows the proposed metal-cavity nanopillar structure coupled by an evanescent field to an InP-membrane waveguide [1]. Both the laser and waveguide are fabricated in a III-V layer stack bonded to a silicon substrate with BCB [2]. The pillar has an undercut above and below the active region (InGaAs) to increase the cavity quality factor, however we did not consider any pillar undercut for the actual fabrication of devices. The pillar is covered by a dielectric layer and then encapsulated with silver to form the metal-cavity. The metal cladding makes electric contact on the top of the pillar, whereas a lateral p-contact is deployed over a large area to minimize its contact resistance. For characterization purposes, we include a grating coupler to couple the light out of the chip.

This report is organized as follows. The bonding process of III-V to silicon is briefly described in the second section. The third section discusses the main technology that has been specifically developed for the fabrication of the nanostructures involved. The fourth section shows step-by-step the process flow that has been designed for the full fabrication of the laser device. Finally, some conclusions are presented.

2. Bonding process

The bonding process of III-V to silicon is carried out to get high refractive index contrast between InP and the bonding layer (BCB, n = 1.45). This is required to fabricate waveguides that are narrow (typically 400 nm wide) and support a single propagating mode at 1.55 μm. Such narrow waveguides are needed to minimize the mode mismatch between the nanolaser and the output waveguide.

The bonding itself is carried out with BCB, however, for technological reasons, SiO_x is deposited on both the III-V and silicon wafers before BCB is spun and cured. Furthermore, according to the design of typical grating couplers which rely on the back-reflection of the downward diffraction, the full bonding layerstack (SiO_x/BCB/SiO_x) must be 1.9 μm to maximize the chip-to-fiber coupling efficiency. In order to minimize outgassing effects during high temperature processes like annealing, we carry out thick bonding (i.e. 700 nm thick BCB).

The main issues that can arise during the bonding process are: the non-uniformity of the bonding layerstack which can compromise the coupling efficiency, and semiconductor growth defects of the III-V wafer, which depending of their size could lead to the failure of the bonding process.

3. Technology development

3.1. Electron-beam lithography and etching processes

The definition of the nanostructure is carried out by electron-beam lithography (EBL) due to the high resolution required. This is done in three EBL steps. During the first lithography, the nanopillar is defined. Later, an overlay exposure is needed to define the waveguide and, finally, the grating coupler is defined with another overlay exposure. Three different lithographic masking schemes are used during these EBL steps, which are depicted in Fig. 2 and discussed in the following.

The first EBL exposure is done using HSQ resist, which is a negative resist well known for its usage in high resolution lithography [3]. Since it can be thinner than 100 nm, the influence of the electron scattering inside the resist is limited. Nevertheless, its thickness is not enough to etch a hardmask able to withstand the etching of the pillar (about one micrometer high), and therefore it has to be used in combination with another resist in a bilayer resist scheme in order to be able to etch high aspect ratio structures [4]. The pattern in HSQ is transferred to an underlying HPR504 resist by means of a reactive-ion-etching (RIE) process using oxygen, which in turn is used to transfer the pattern into a SiO_x layer with a CHF_3-based RIE. Finally, the SiO_x is used as a hardmask to etch the semiconductor pillar using inductively coupled plasma RIE (ICP-RIE) using a methane-hydrogen chemistry (CH_4:H_2).

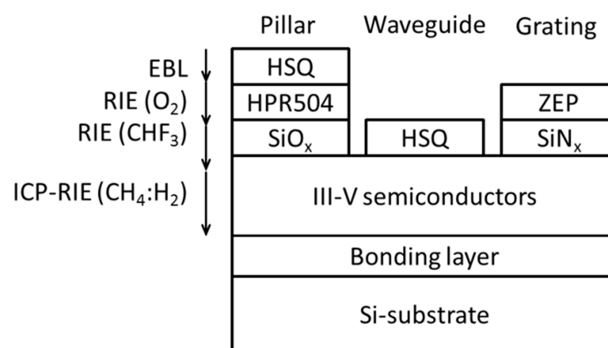


Figure 2. Processing schemes to fabricate the nanostructures. The top layer of each lithographic scheme is always defined by EBL and development.

In a second EBL exposure, the waveguide is defined at the bottom of the pillar structure. During this step, a mask protection for the pillar is mandatory, otherwise the pillar will be eroded during the waveguides etching. For this purpose, the hardmask to etch the pillar is not removed after the first lithography.

An overlay EBL normally demands a prior planarization of the surface to keep the resist thickness uniform as well as the hardmask layer. We avoid such planarization by using the HSQ resist directly as the hardmask. This technique requires enhancing the resistance of HSQ to the semiconductor etching chemistry used in the RIE, what can be done either by curing HSQ [5] or by treating it with an oxygen plasma [6]. In this way, after the pillars have been etched, HSQ is spun, e-beam exposed, developed, and treated with an O_2-plasma. Later, this HSQ is used as the hardmask to etch the waveguide using methane hydrogen in a RIE process. The result of these two lithography steps is shown in Fig. 3a to Fig. 3b.

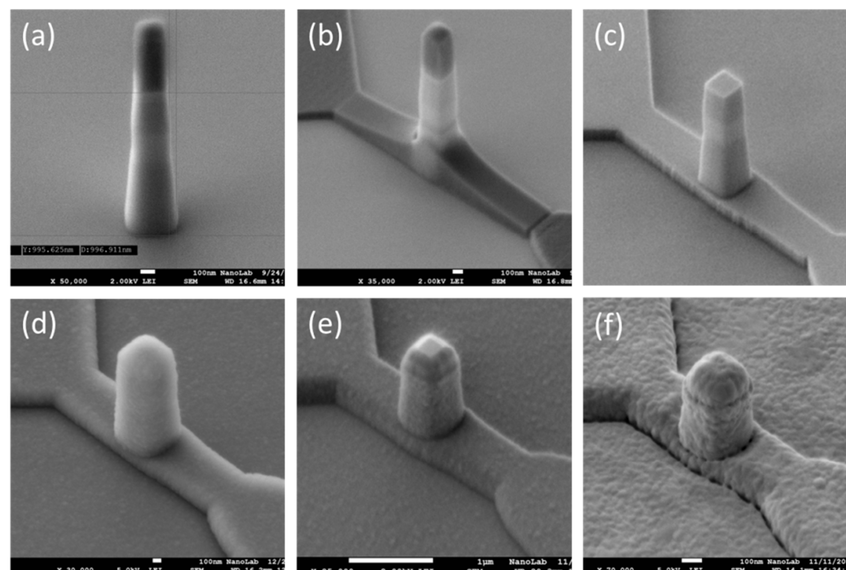


Figure 3. (a) Pillar after first etching (b) After HSQ resist development. (c) After waveguide etching and removal of masking layers. (d) After SiO2 deposition. (e) After etching of SiO2 from pillar top. (d) After Ge/Ag deposition to form the metallo-dielectric cavity.

A final e-beam lithography is required to fabricate the grating coupler. In this case, ZEP resist in combination with a SiN_x mask is used. This is preferred because it is a positive resist, which means that any non-exposed region (i.e. the pillar and waveguide) will be protected by the SiN_x hardmask during the grating etching. The undercut to enhance the quality factor of the cavity, as described in our laser design [1], can be fabricated right after the pillar etching by a selective wet etching of InP, nevertheless we do not include this fabrication step in our current process.

After the nanostructures have been fabricated with EBL, dielectric and metallic layers are deposited to form the metallo-dielectric cavity and do the metallization of the device in order to complete the fabrication as shown in Fig. 3b. These steps are discussed in the following (section 3.2).

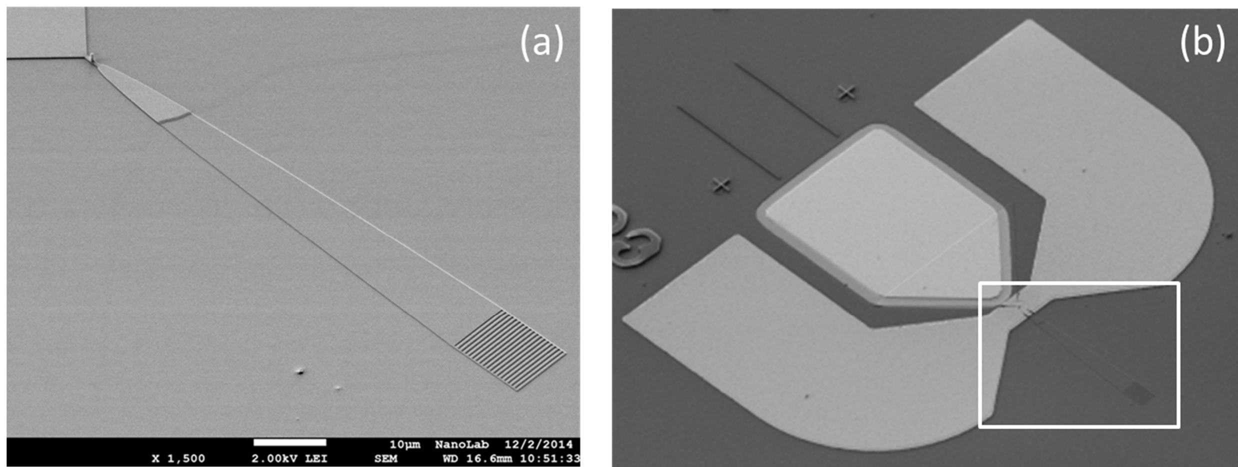


Fig. 3. (a) Panoramic view after the pillar, waveguide and grating coupler fabrication by three e-beam lithography steps. This device region corresponds to the region indicated in Fig. 3b with a white square. (b) Panoramic view after metallization of the device.

3.2. Deposition of dielectrics and metals

The metal cladding of the cavity would create a short circuit unless a dielectric layer is deposited before silver, which also helps to reduce the metal loss according to the design [1]. For this purpose, either Si_xN_x or SiO_x can be deposited by plasma-enhanced chemical vapor deposition (PECVD), however it has been found that a SiO_x cladding would result in a higher quality factor due to its lower refractive index. Before the actual deposition of the chosen dielectric, a thin passivation layer of SiN_x of a few nanometers can be deposited at low temperatures to reduce the surface recombination [7]. Since the resonant wavelength is mainly given by the cavity size (thickness of the dielectric cladding plus the semiconductor pillar width), it is important to consider that the PECVD deposition rate on sidewalls is about two thirds of the deposition rate on a flat surface. Figure 3d shows the pillar after the deposition of SiO_x.

After the pillar has been covered with a dielectric layer, silver can be thermally evaporated to form the metal-cavity. However, since silver does not stick on SiO_x/Si_xN_x, an adhesion layer must be previously deposited by lift-off, for example Ti/Au [8], chromium [9] or germanium. In order to properly cover the sidewalls of the pillar, the silver evaporation should be done at different angles. Moreover, since the evaporation leads to the formation of silver grains, rapid thermal annealing (RTA) is applied after the evaporation to increase the metal grain size resulting in a more uniform metal with reduced scattering loss. Figure 3f shows the pillar covered with silver after RTA.

4. Fabrication process flow

➢ **Initial layerstack**

- Initial layerstack after BCB bonding

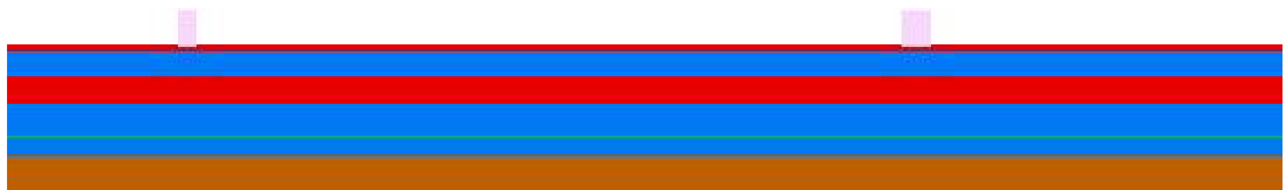
➢ **Removal of protection layers**

- The photoresist is removed with acetone and the InP protection layer is wetly etched with H_3PO_4

➢ **Deposition of hardmask, HSQ resist and EBL exposure**

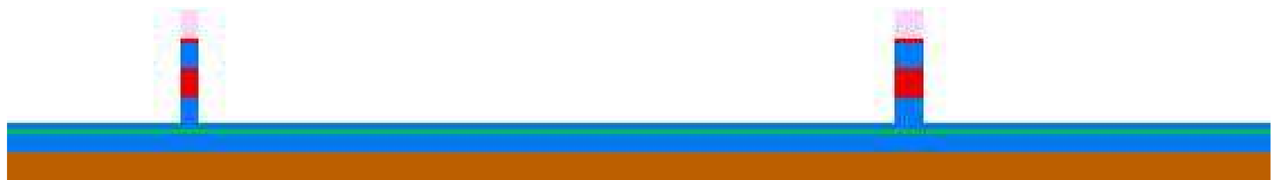
- A SiO_x hardmask (440 nm thick) is deposited by PECVD
- HPR504 photoresist (400 nm) is spun. This intermediate layer is required to transfer the pattern from the EBL resist (HSQ) into the SiO_x hardmask
- HSQ resist (100 nm) is spun and finally a thin layer of gold is deposited to be able to focus on HSQ during the lithography
- The EBL to define the nanopillars is carried out

➢ **Polymer RIE and silicon-oxide RIE**



- After EBL exposure, the HSQ is developed with a MaD531S solution. In the figure, the left side pattern corresponds to the transversal cross section of the pillar, whereas the pattern at the right is the longitudinal cross section. In later steps, the difference between these cross sections is more clear.
- The HSQ pattern is used as mask to etch the pattern into HPR504 with a RIE process using an O_2-plasma.
- The pattern is transferred to SiO_x using a CHF_3 chemistry in a RIE process
- The remaining HSQ and HPR504 resists are cleaned

➢ **Etching of nanopillars by ICP-RIE**

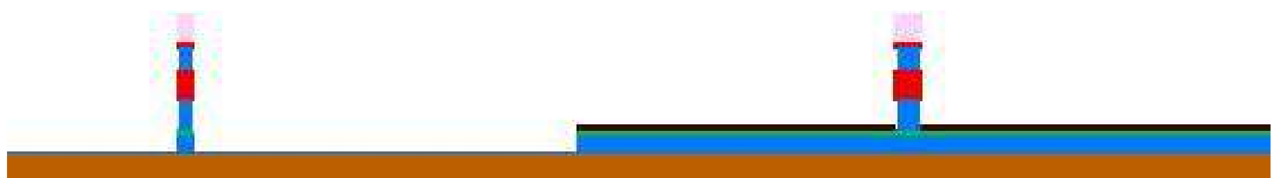


- The nanopillars are etched using CH_4-H_2 in ICP-RIE

➢ **Fabrication of undercut fabrication by wet etching**

- The etchant H_3PO_4:HCl is used to create an undercut in the pillar by selective wet ething of InP. During the same step, the quaternary layer (InGaAsP) is reached.

➢ **EBL exposure of waveguides and etching**



- HSQ resist (100 nm) is spun and exposed with EBL
- The wavegides pattern is developed with a MaD531S developer
- The waveguides are etched with ICP-RIE using CH_4-H_2

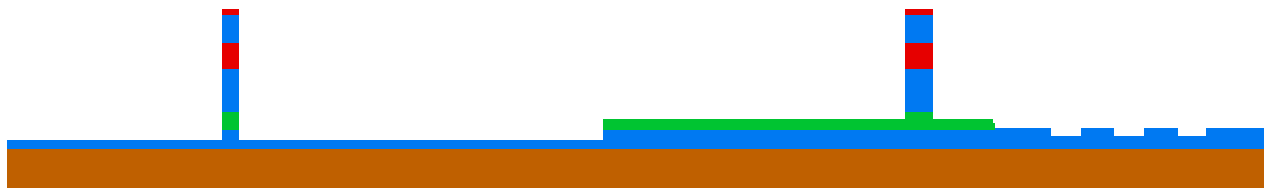
➢ **Optical lithography to remove quaternary**

- AZ4533 resist is spun and exposed by optical lithography
- AZ4533 is developed with MaD531S
- Quaternary (InGaAs, green layer) is removed by wet etching form top of waveguide

➢ **EBL exposure of grating coupler and etching**

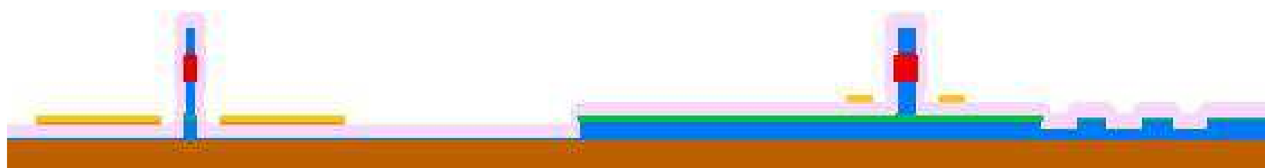
- A Si_3N_4 layer is deposited by PECVD
- ZEP resist (300 nm) is spun and exposed with EBL to write the grating coupler
- The ZEP pattern is developed with developer n-Amyl Acetaat
- The pattern is transferred to the Si_3N_4 by a RIE process
- An optical lithography is done using AZ4533 to protect the pillar

➢ **Etching of gratings with RIE**



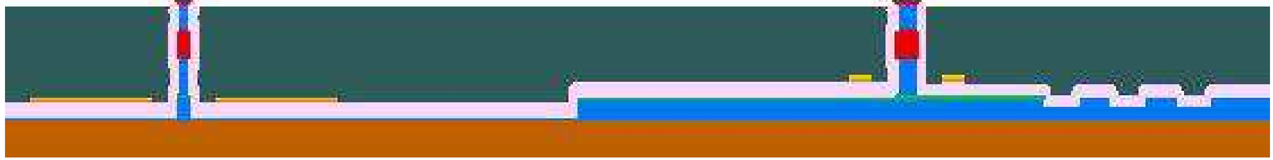
- The grating pattern is etched into the semiconductor using a RIE process and the Si_3N_4 hardmask is removed

➢ **Deposition of adhesion pad**



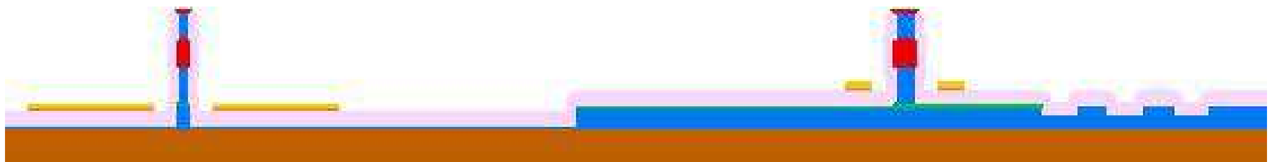
- A SiO_x layer 175 nm thicks is deposited by PECVD
- An adhesion layer consisting of Ti/Au (50/40 nm) is deposited next to the pillar with lift-off. This adhesion pad is required to keep the silver in place later on, when it is deposited

➢ **Planarization and etching of SiO_x cladding**



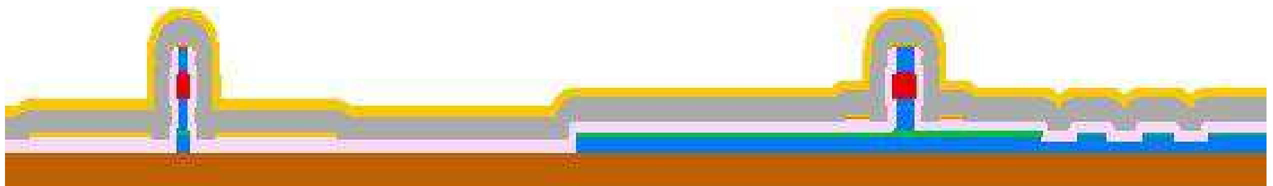
- The sample is planarised by spinning MaN440 resist and developing it back with a water-diluted MaN531S solution.
- Once the pillar top is exposed, the SiO_x is etched with Nitride RIE using CHF_3:O_2

➢ **Removal of MaN440 photoresist**



- The photoresist MaN440 is removed with acetone

➢ **Deposition of metals to form metal-cavity**

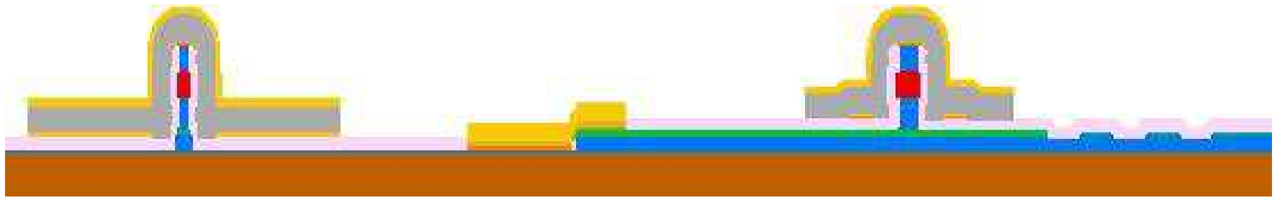


- A few nanometers (4 nm) of Germanium are deposited by thermal evaporation
- A 200 nm thick silver is deposited by thermal evaporation
- The silver quality is improved by rapid thermal annealing at 400 C°
- A second layer of silver is deposited
- A thin layer (100 nm) of gold is sputtered to prevent silver oxidation

➢ **Optical lithography to protect pillars from metals etching**

- AZ4533 optical resist is spun and exposed with optical lithography. This step is done to protect the pillar and n-contacts during the wet etching of gold and silver
- The AZ4533 resist is developed with MaD531S
- The gold and silver are etched wetly with a KCN solution

➢ **Evaporation of p-contact**



- MaN440 resist is spun, exposed and developed
- SiOx is etched with BHF
- The p-contact (Ti/Pt/Au) is deposited in a lift-off process
- The fabrication is finished

5. Conclusions

The main technology developed to fabricate waveguide-coupled nanocavities has been described in this report. In addition, the process flow was presented step-by-step to provide the reader a detailed description of the fabrication process. The proposed fabrication has been used to demonstrate nanoLEDs. Furthermore, the technology reported is relevant also for other metal-based nanophotonic circuits.

References

[1] V. Dolores-Calzadilla, et al., “Metallo-dielectric nanolaser coupled to an InP-membrane waveguide”, 17th Annual Symposium of the IEEE Photonics Benelux Chapter, 2012.

[2] J. van der Tol, *et al.*, “Photonic integration in Indium-Phosphide Membranes on Silicon (IMOS)”, IET Optoelectronics, 5(5), pp. 218–225, 2011.

[3] A. E. Grigorescu and C. W. Hagen, “Resists for sub-20-nm electron beam lithography with focus on HSQ: state of the art”, Nanotechnology, 20(29), pp. 1-30, 2009.

[4] F. van Delft, *et al.*, “Hydrogen silsesquioxane/novolak bilayer resist for high aspect ratio nanoscale electron-beam lithography”, J. Vac. Sci. Technol. B 18(6), pp. 3419-3423, 2000.

[5] L. O’Faolain, *et al.*, “Fabrication of photonic crystals using a spin-coated hydrogen silsesquioxane hard mask”, J. Vac. Sci. Technol. B 24(1), pp. 336-339, 2006.

[6] M. Carette, “Simple technological process for the fabrication of optical InP nanowires integrated into a benzocyclobutene matrix”, Journees Nationales sur les Technologies Emergentes en Micronanofabrication, 2008.

[7] J. Kim, *et al.*, “RPCVD Silicon Nitride Passivation on InGaAsP with Temperature Ramping during Deposition”, 207th Electrochemical Society Meeting, pp. 361-366, 2005.

[8] J. Hyoung Lee, “Electrically pumped sub-wavelength metallo-dielectric pedestal pillar lasers”, Optics Express 19(22), pp. 21524-21531, 2011.

[9] M. T. Hill, *et al.*, “Lasing in metallic-coated nanocavities”, Nature Photonics, 1(10), pp. 589–594, 2007.