Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Report on Fabrication of Modulators

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Executive Summary

This is a report on fabrication of NAVOLCHI phase and absorption modulators. In Chapter 1, we introduce the working principle of the plasmonic phase modulator and give the target design of individual modulators. The mask design of the silicon-on-insulator (SOI) die submitted to ePIXfab is presented in section 1.1, followed by the discussion of the fabrication process flow which has been carried out as a post-processing step for defining the phase modulators.

In Chapter 2, we similarly report on fabrication of the plasmonic absorption modulator.

Both modulators have been successfully fabricated and tested. The results have already been published in several journal and conference contributions.

Change Records

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Background

Two modulator structures have been successfully fabricated within NAVOLCHI - namely the surface plasmon polariton absorption modulator [1,2], where the intensity of SPP is directly modulated by plasma effect in metal oxide, and surface plasmon polariton phase modulator [3,4], where the phase of SPP is modulated making use of the Pockels effect, see Figure 1.

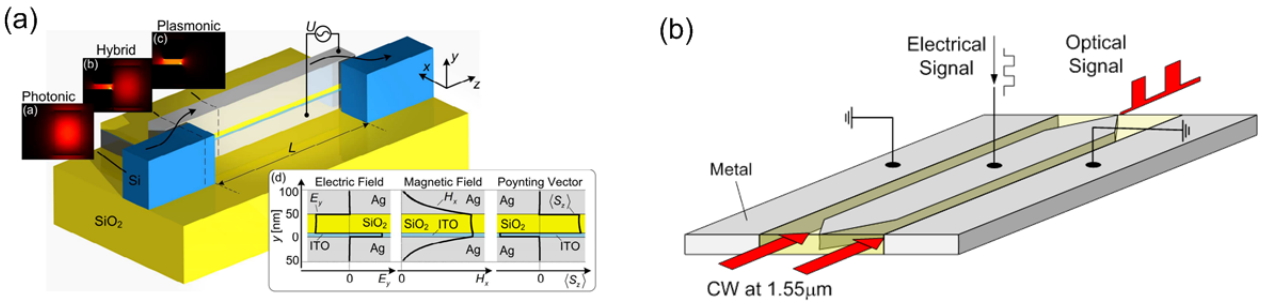

Figure 1 Plasmonic modulator approaches engaged by NAVOLCHI. (a) Surface plasmon polariton absorption modulator [1,2] and (b) plasmonic phase modulator[3,4].

In this deliverable, we discuss the design of the modulators to be fabricated. We describe the fabrication processes which have been carried out for fabrication of the absorption and phase modulators. We report the exact geometry of the fabricated devices. In the last part of this deliverable, we shortly discuss the next steps that will be carried out for improving the performance of the current modulators.

1. Plasmonics phase modulator

We have successfully fabricated two generations of plasmonic phase modulators, which show ultrawide RF and optical bandwidths. The modulators are tested for up to 40Gbit/s data modulations and the results are accepted for publication in Nature Photonics [4].

Plasmonic phase modulator comprises two metal electrodes separated by nanometer scale slot which is filled with an electro-optic polymer. Cross section of the device is given in Figure 2. At the 1550nm wavelength, such plasmonic slot waveguide sustains gap surface plasmon polariton (SPP) mode which is strongly confined in the slot as can be seen in Figure 2. By applying a voltage between the metal electrodes, the refractive index of the electro-optic polymer can be modulated, which consequently results in modulation of SPP phase.

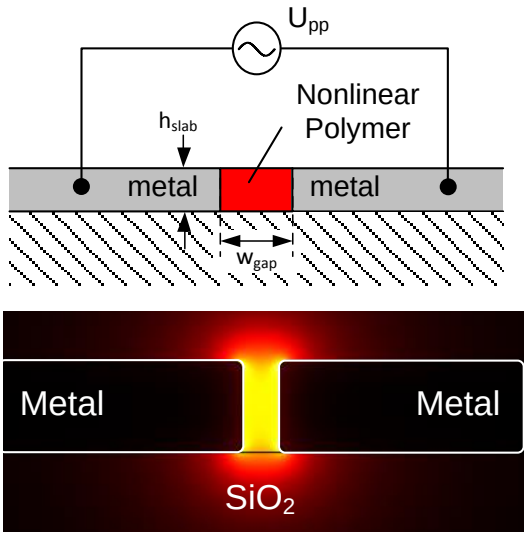

Figure 2 Cross section of the plasmonic phase modulator

A promising approach to couple light from a silicon nanowire to a plasmonic slot waveguide, we found to be the tapered metallic coupling configuration which provides very large and broadband coupling efficiency[5]. Performance optimization of the device can be found in NAVOLCHI **Milestone 25**. In such a coupling scheme, quasi-TE polarized light guided through silicon nanowire is adiabatically squeezed and launched into the plasmonic slot waveguide, see Figure 3.

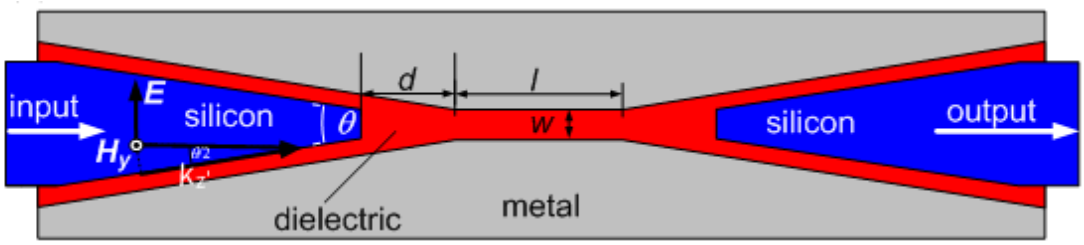

Figure 3 Top view of the mode convert to convert the photonic silicon nanowire mode to gap SPP at the plasmonic slot.

The fabrication of single plasmonic phase modulator has been successfully carried out by IMEC and KIT, by dividing the entire fabrication process flow into three steps

- Mask design for the fabrication of silicon/plasmonic platform
- Fabrication of passive silicon on insulator (SOI) chips at IMEC
- Fabrication of active plasmonic parts at KIT

1.1 Mask design

KIT has designed a mask for the fabrication of the passive silicon platform, which should be farther post-processed in order to define the metallic parts of the modulator. The entire mask layout occupies 3 × 3 mm^2 area, see Figure 4. Silicon nanowires have been designed with a width of 450nm. Two standard diffraction grating couplers are used to couple light in and out the silicon nanowire waveguides. The important parts of the mask are the silicon taper pairs with various separations from 2 μm to 45 μm, see Figure 5. The silicon tapers have tapering angle of 15˚ and tip size of 120 nm, see **Milestone 25** "*Decision on optimized plasmonic waveguide couplers*".

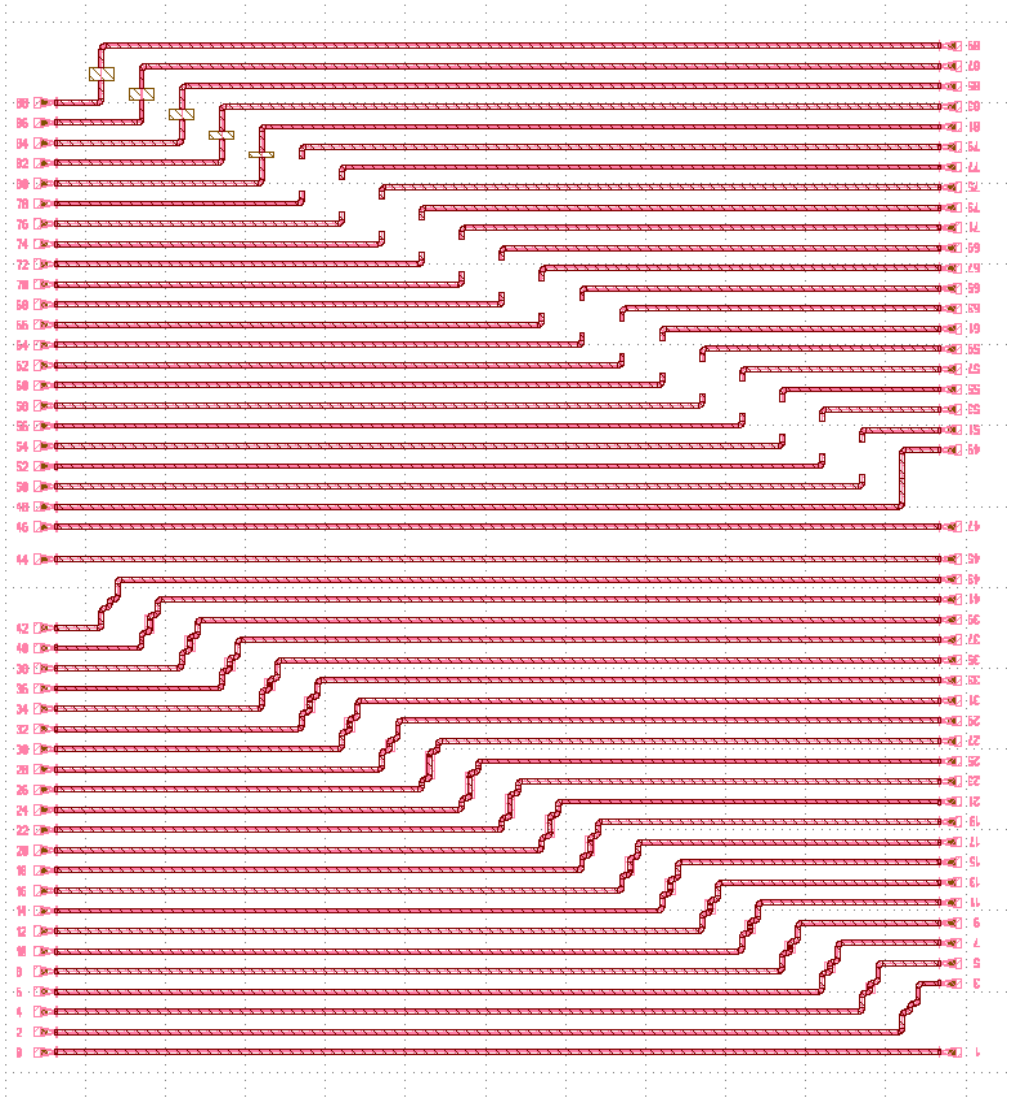

Figure 4 The entire mask used for fabrication of the passive silicon part of the plasmonic modulator. This comprises diffraction gratings, silicon nanowires and silicon tapers.

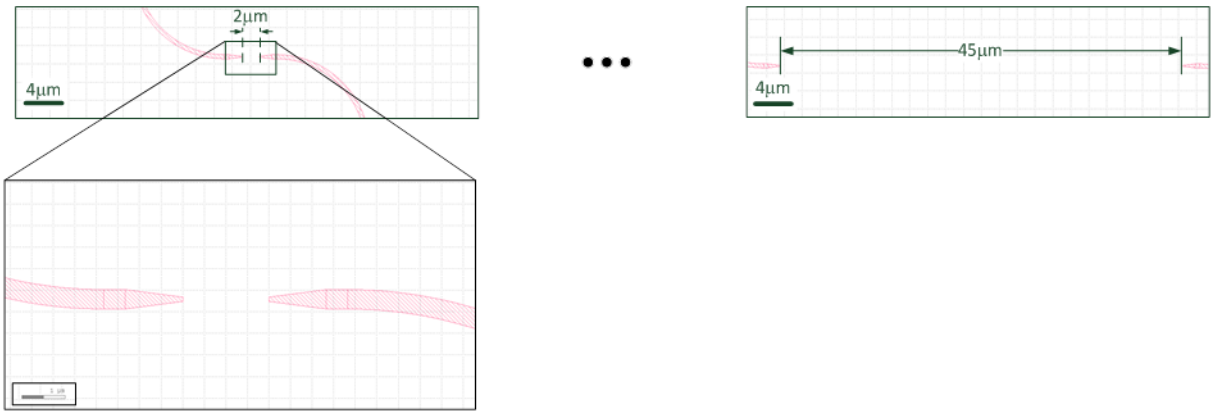

Figure 5 Silicon tapers designed for the fabrication of plasmonic modulator

1.2 Fabrication methods

The entire fabrication process flow for the phase modulator is given in Figure 6. Silicon on insulator (SOI) wafer with a buried oxide layer thickness of 2 µm has been processed by IMEC. Si nanowire waveguides with a height of 220 nm and a width of 450 nm are fabricated on a silicon on insulator (SOI). A 193 nm DUV lithography is used followed by Si dry etching. Silicon tapers with a taper angle of 15˚ and a tip size of 120 nm are structured in the final etching process. The metallic slot waveguides are fabricated by a standard lift-off process with PMMA e-beam resist. A 150 nm thick gold layer is evaporated onto the samples by an electron beam evaporation system. After completing the lift-off process the samples are coated with the commercially available polymer M3 having a maximum electro-optic coefficient of r_{33} = 70 pm / V [6]. The electro-optic property of the polymer is then activated by a poling procedure, where a static electric field aligns the randomly oriented dipole moments of the chromophores at an elevated temperature [7]. After rapid cooling to room temperature, the ordering of the dipole moments pertains even after removal of the electric field.

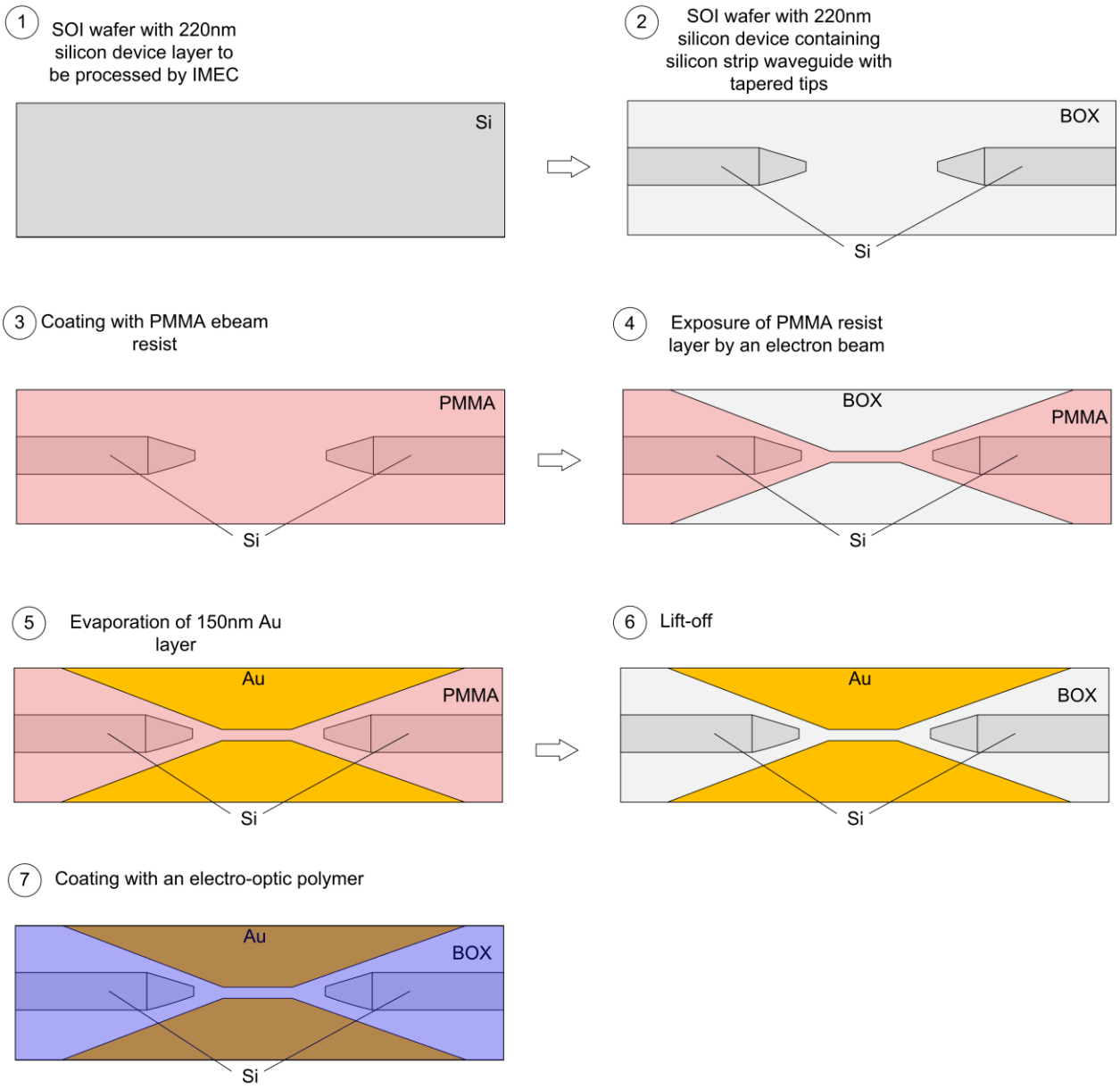

Figure 6 Fabrication process flow for defining the metallic slot.

1.3 Fabricated devices

Figure 7 gives a scanning electron microscope (SEM) image of the silicon nanowire waveguide fabricated by IMEC. The fabricated silicon tapers that are used for a gap SPP excitation are given in the Figure 8.

KIT fabricated two generations of plasmonic phase modulators applying to the above mentioned process flow. The first generation (1stG) of modulator has been fabricated in a ground-signal-ground (GSG) configuration with metallic slots, having a length of 34 μm and a slot width of 200 nm, on each side of the signal electrode. In the second generation (2ndG) phase modulator, we improved the fabrication process and, thereby, reducing the slot size down to 140 nm, and the modulator length to 29 μm. The 2ndG device was designed to have a ground - signal (GS)

configuration. A scanning electron microscope (SEM) picture of the 1stG device before coating with an electro-optic polymer is shown in Figure 9[3,4].

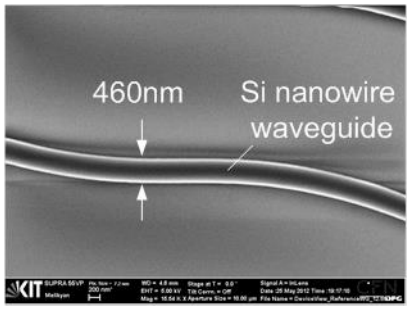

Figure 7 Scanning electron microscope image of the fabricated silicon nanowire waveguide

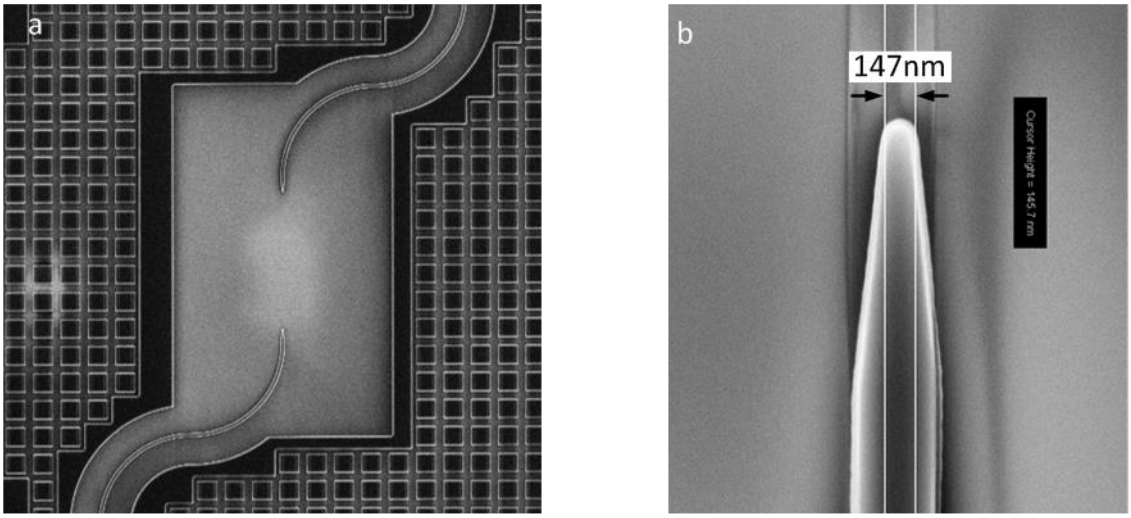

Figure 8 Fabricated passive silicon platform. (a) Fabricated pair silicon tapers which will be used for light coupling in and out from the plasmonic modulator. (b) Fabricated silicon taper. Designed tip size of 120 nm resulted in 150 nm tip size.

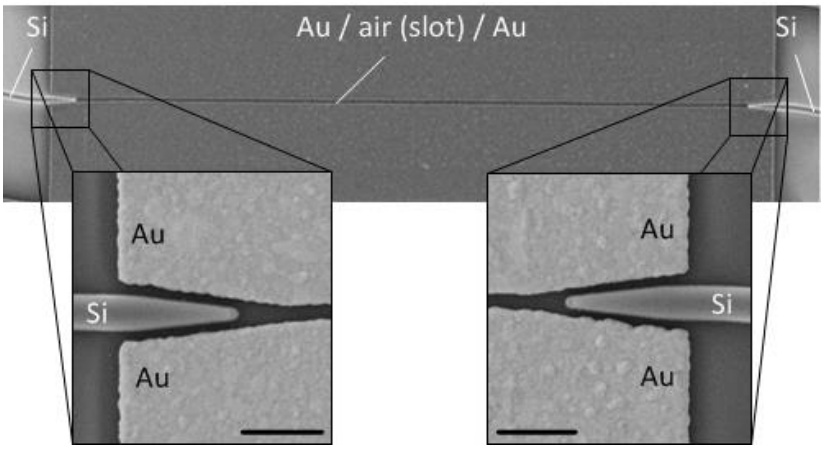

Figure 9 Scanning electron microscope image of the fabricated plasmonic phase modulator. The photograph is taken before coating with an electrooptic polymer. Black bars are one micrometre.

2. Plasmonic absorption modulator

We have successfully fabricated the first generation of plasmonic absorption modulators which already show good switching behaviour with an extinction ratio of 6dB for 3V applied voltage. The results have been submitted to CLEO2014[2].

The surface plasmon polariton absorption modulator (SPPAM) is designed on a standard silicon-on-insulator (SOI) platform. The core of the device is the active material indium-tin-oxide (ITO), since the carrier density and thus, the absorption of ITO may be switched by applying an electrical field. The modulator comprises a metal-oxide-ITO-silicon layer stack guiding a hybrid surface plasmon polariton, see Figure 10.

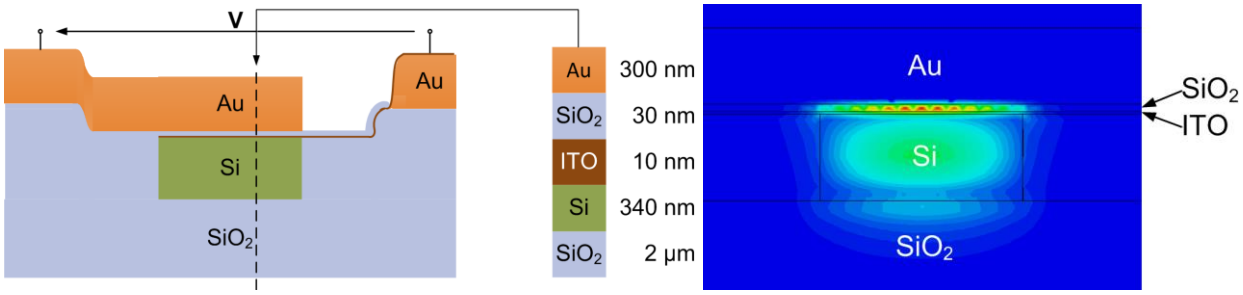

Figure 10 Cross section of the plasmonic absorption modulator comprising a metal-oxide-ITO-silicon layer stack and the plasmonic hybrid mode in the modulator section.

In this device, light is coupled to the hybrid plasmonic mode via a photonic silicon strip waveguide with a height of 340 nm, see Figure 11. For switching, an electric field is applied by means of 150 nm thick gold electrodes. The top electrode is provided by the top metal of the plasmonic waveguide. The bottom electrode is contacting the 10 nm thick ITO layer. A silicon oxide layer of 20 nm thickness is sandwiched between the ITO and the top metal layer as an insulator layer preventing the leaking currents.

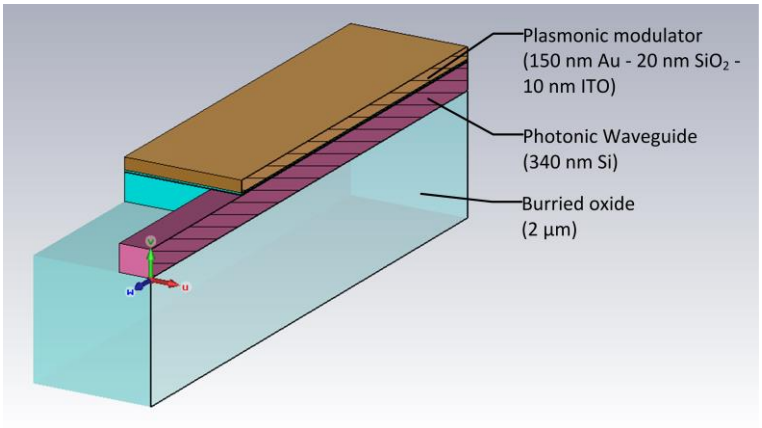

Figure 11 Design of the surface plasmon polariton absorption modulator on SOI platform. Light guided through the photonic silicon nanowire waveguide excites the plasmonic hybrid mode in the metallic section. Voltage is applied between ITO and top gold layer in order to modulate the absorption experienced by the SPP

2.1 Mask design

The mask layout for the SPPAM comprises modulator of various device lengths (3 µm, 5 µm, 10 µm and 20 µm). Besides single devices, there are modulator arrays of two and four channels with pitches of 35 µm, 50 µm and 250 µm. Furthermore, the layout includes purely passive devices to determine the corresponding losses.

Figure 12 shows a modulator array with four channels. The red areas are the passive silicon components. All passive devices are designed for a height of 340 nm and TM polarized light. They can be fabricated in a single etch step. The light is coupled to the chip via grating couplers (GC, period 840 nm, fillfactor 0.6). It is then guided by 800 nm wide waveguides and split into several arms with multimode interference (MMI) devices of 8.39 µm length. The modulators are electrically contacted by means of gold pads (60 µm x 100 µm), indicated by the blue areas.

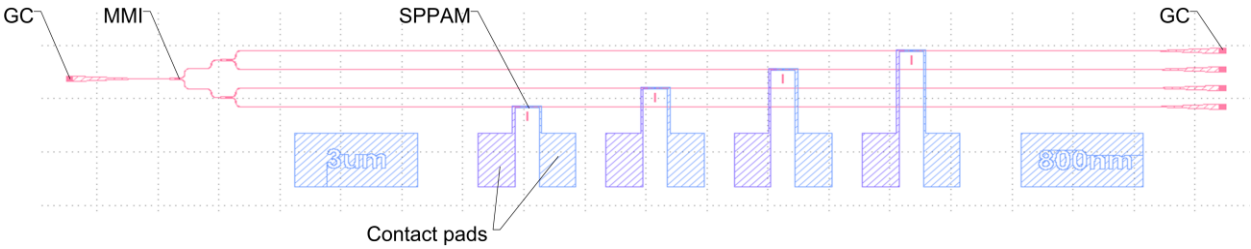

Figure 12 Mask layout for the fabrication of an SPPAM array on an SOI platform

2.2 Fabrication methods

The fabrication process is shown in. The first step was the fabrication of the passive silicon devices on a SOI wafer with buried oxide and silicon device layer thicknesses of 2 µm and 340 nm, respectively. All passive devices were fabricated in a single e-beam lithography and ICP etching step. Next, a 500 nm thick SiO_2 cladding was deposited with PECVD. This oxide was opened in the following step (photo lithography and RIE etching) to access the underlying silicon waveguide. Then, 10 nm of ITO were deposited on top of the silicon waveguide (photo lithography and sputtering). To contact the ITO layer the 150 nm thick bottom electrode was deposited via photo lithography and e-beam evaporation. For the photo lithography, the same mask as for the ITO deposition was used, but shifted away from the silicon waveguide. After that, a 20 nm thin SiO_2 layer was deposited with e-beam evaporation. This was followed by the deposition of the top electrode. Finally, the oxide was opened to access the bottom electrode.

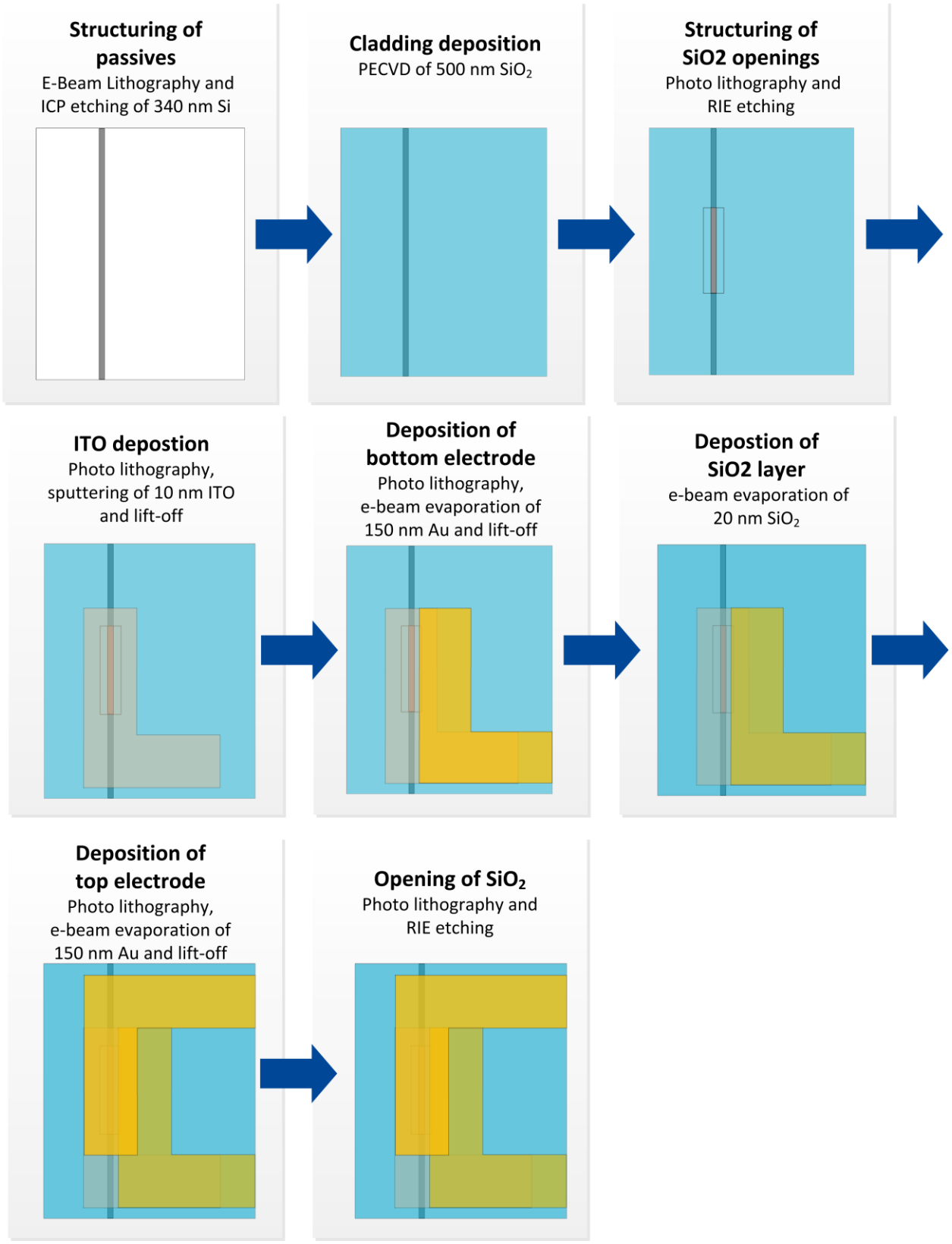

Figure 13 Fabrication process of the SPPAM

2.3 Fabricated devices

Figure 14 shows an optical microscope image of fabricated modulator arrays with four channels and various device lengths. A close-up of a 5 µm long single device can be seen in Figure 15. The SEM image given in Figure 16, shows a cross section of the SPPAM. The rectangle in the middle is the silicon waveguide with the thin—and therefore barely visible—ITO and SiO_2 layers on top. The bottom electrode is shifted with respect to the top electrode. The trenches are caused by the fact that the cladding deposition on top of the silicon waveguide leads to a bump in the oxide layer. This bump is transferred when opening the oxide in the following step.

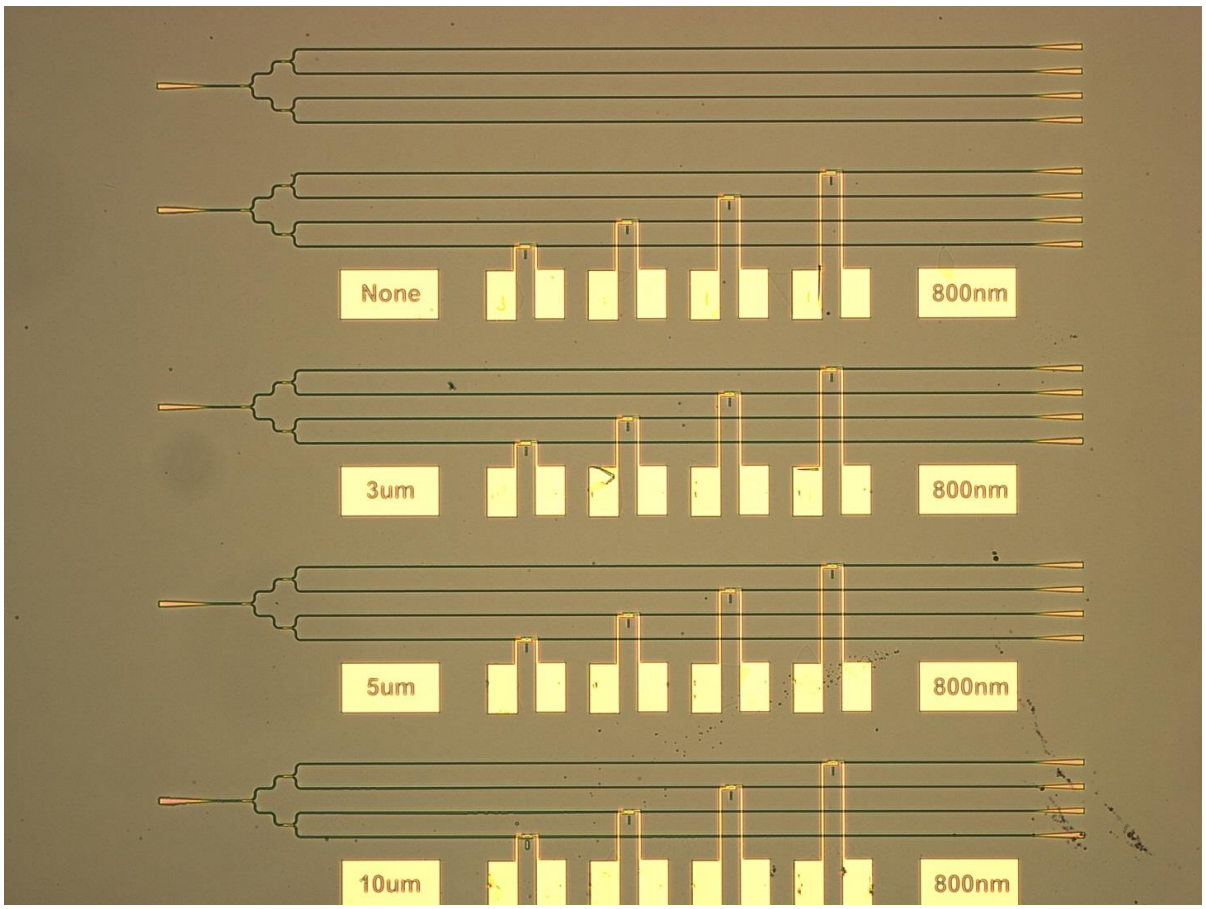

Figure 14 Optical microscope image of fabricated SPPAM arrays with various device lengths

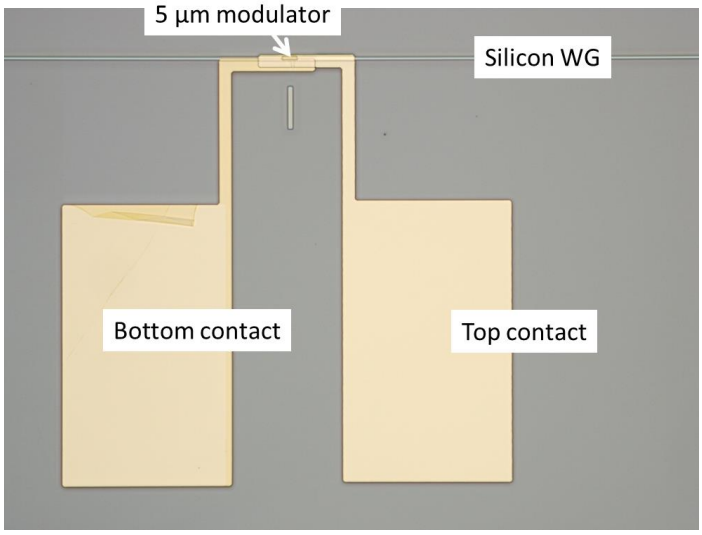

Figure 15 Optical microscope image of a 5 µm long SPPAM

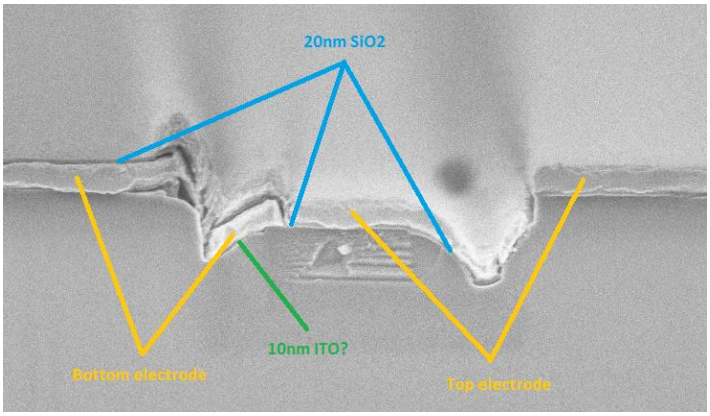

Figure 16 Cross section of a fabricated SPPAM (SEM image)

3. Outlook

3.1 Phase modulator

Eventually, we aim to combine two phase modulators in a Mach-Zehnder-Interferometer (MZI) configuration to convert a phase modulated SPP signal into an intensity modulated signal. The mask of the passive silicon platform for the MZI modulators is finalized by KIT and has been submitted to IMEC. IMEC will ship already processed wafer in the middle of February 2014 to KIT. KIT then will carry out the following activities during the next 6 month:

- Optimizing the modulator fabrication in MZI configuration
- Fabricating the plasmonic MZI modulators
- Characterizing the MZI modulator performance for data modulation.

3.2 Absorption modulator

Based on the first characterization results, several fabrication issues have been identified. To solve them we will particularly need to

- Improve the quality of 20nm thick silicon dioxide insulator layer
- Reduce the silicon dioxide layer thickness in order to increase the accumulation layer inside ITO
- Improve the coupling scheme between silicon nanowire and plasmonic hybrid mode
- To improve the electrical contact to the ITO layer

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