Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Report on characterization results of all optical interface plasmonic passive components

Deliverable no.: D6.2
Due date: 01/01/2014
Actual Submission date: 07/31/2014
Authors: KIT
Work package(s): WP6
Distribution level: RE[1] (NAVOLCHI Consortium)
Nature: document, available online in the restricted area of the NAVOLCHI webpage

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Deliverable Responsible

Organization: Karlsruhe Institute of Technology
Contact Person: Argishti Melikyan
Address: Institute of Microstructure Technology
Hermann-von-Helmholtz-Platz 1, Building 321
76344 Eggenstein-Leopoldshafen
Germany
Phone: +49 (0)721 – 608 42496
Fax: +49 (0)721 – 608 26667
E-mail: argishti.melikyan@kit.edu

Executive Summary

In this deliverable, we compare two scenarios of photonic-die packaging, namely, 2D in-plane packaging and 3D vertical stacking. Examining the advantages and disadvantages for both cases, we conclude that the 2D in-plane packaging is the most realistic scenario which can be applied in the NAVOLCHI's final interconnects system.

Change Records

Version	Date	Changes	Author
0.1 (draft)	2014-10-07	Start	A. Melikyan
1 (submission)	2014-10-07		A. Melikyan

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1 Introduction

NAVOLCHI's interconnect physical layer employs plasmonic devices to realized parallel four-channel high speed optical link between electronic dies within a system-in-package. Two possible packaging scenarios are given in Figure 1.1. In the case of the 2D packaging, the dies are horizontally placed side-by-side either on a common or a separate PCB carrier board. Contrary, 3D vertical stacking eliminates the need of the fiber optical cables between the dies and uses a free space communication channel between the dies. In this case, electronic dies should be flip-chip stacked in the vertical direction.

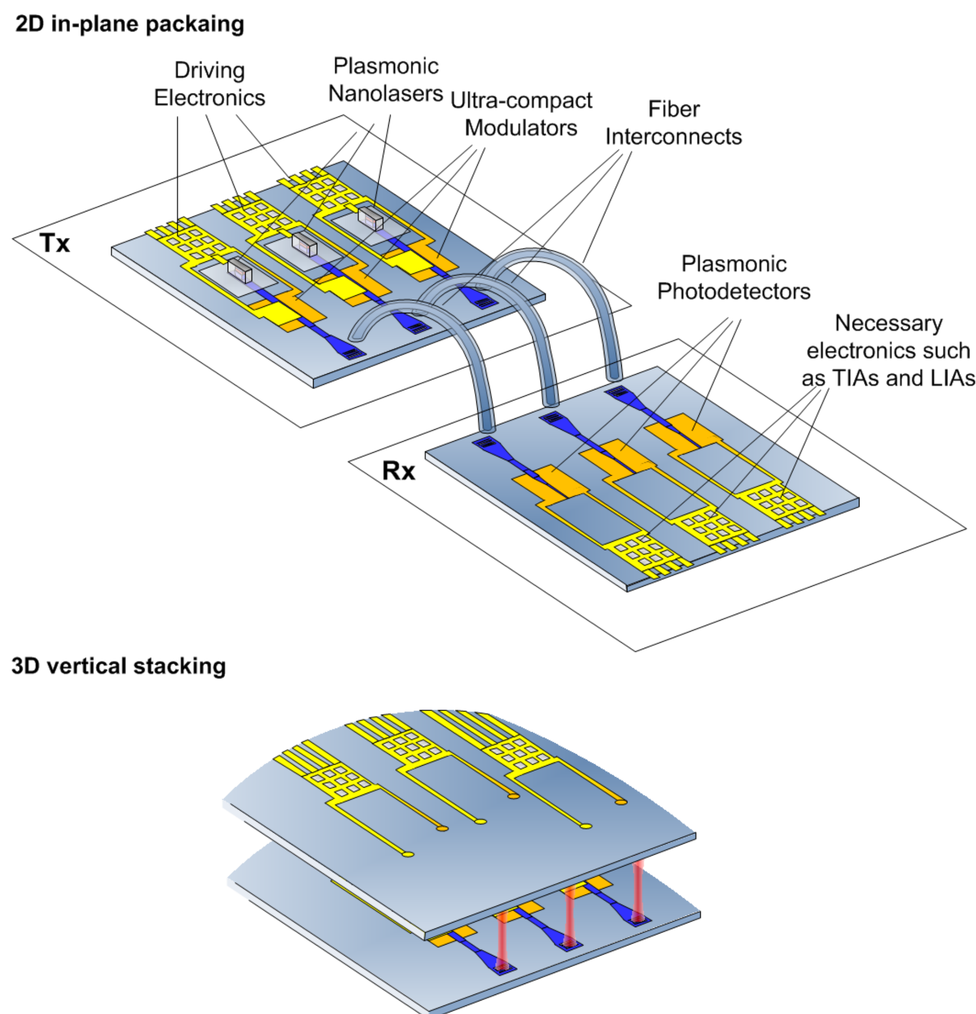

Figure 1.1 Two packaging architectures considered in NAVOLCHI

NAVOLCHI plasmonic interconnect physical layer comprises plasmonic lasers, modulators, amplifier, detectors The table summarizing the current status of the each of the plasmonic devices is give below

	Design	Fabrication	Static demonstration	High-speed demonstration
Nano-laser	Completed	In progress	Not started	Not started
Modulator	Completed	Completed	Completed	Completed
Amplifier	Completed	In progress	Not started	Not started
Detector	Completed	In progress	Not started	Not started

Figure 1.2 Current status of the plasmonic devices investigated in NAVOLCHI

Because of the delay in fabrications of NAVOLCHI's lasers, amplifiers and detectors, in the current status of the project the most realistic chip-to-chip interconnects architecture that can be realized during the project extension is the NAVOLCHI contingency plan, see Figure 1.3. In this case, light from an external laser is fed to the four plasmonic modulators located on the silicon plasmonic transmitter chip. The light splitting in four channels can be done either off- or on-chip using standard multimode interference (MMI) couplers. All four modulators are driven with electrical signals coming from an FPGA. On the receiver side, IMEC's conventional Si-Ge photodiodes are used to make the optical to electrical signal conversion. The electrical signals after the photodiodes are amplified with the trans-impedance amplifiers and fed into the second FPGA. The received signal quality is analyzed in the second FPGA. Both the transmitter and the receiver chips contain arrays of grating couplers with the required channel pitch of 20…50 µm. Grating arrays on the transmitter and the receiver can be linked either through the fiber arrays [as shown in Figure 1.1(a)] or through the free-space communication channel [in the flip-chip configuration, given in Figure 1.1(b)].

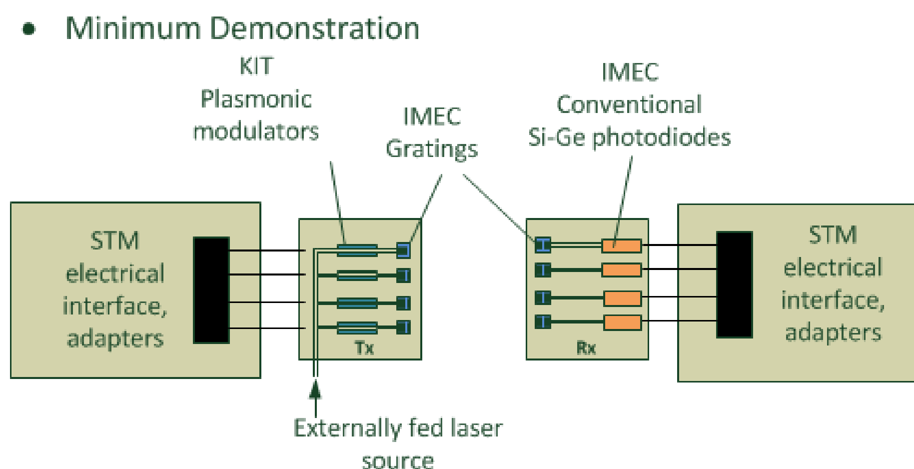

Figure 1.3 The final NAVOLCHI interconnect system

In the following sections, we compare the abovementioned packaging scenarios based on the technological complexities, the required optical power budgets and supported number of channels.

2 2D in-plane packaging

In the case of the 2D in-plane packaging, the channel pitch on the fiber arrays defines the minimum channel pitch on the transmitter and the receiver. Current state-of-the-art fiber arrays provide channel pitch as small as 20 µm…50 µm (*Chiral Photonics, Inc.*). These fiber arrays are available for two configurations of chip-to-fiber coupling, namely, for vertical coupling using grating couplers on the chip and for but-coupling using silicon inverted tapers on the chips, see Figure 2.1.

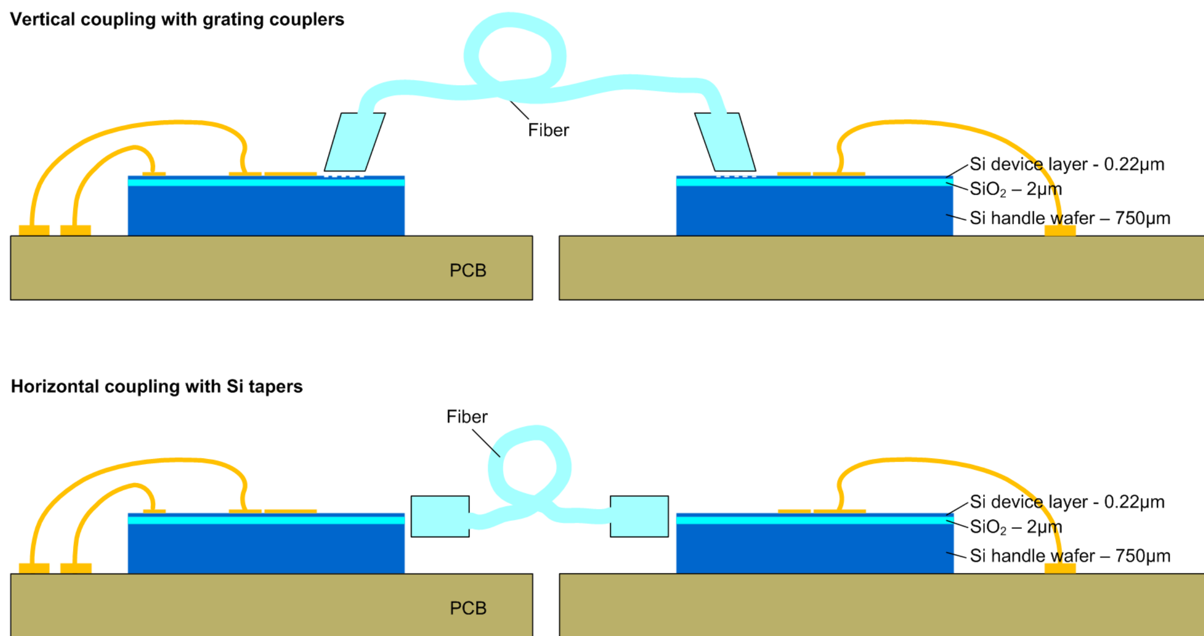

Figure 2.1 2D in-plane packaging with transmitter and receiver chips interconnected with fiber array. (top) Grating couplers are used to couple light vertically in and out of the chips. (bottom) Light is coupled in and out of the fiber array using on-chip silicon inverted taper couplers.

State-of-the-art fiber arrays can be purchased from *Chiral Photonics, Inc.* with channel pitch as small as 20 µm. These arrays are made using *Chiral Photonics'* "Vanishing" central core technology, see Figure 2.2. In addition to the small channel pitch, the fiber arrays by *Chiral Photonics* can also be fabricated with a rectangular channel profile. The rectangular channel profiles within the fiber arrays can significantly reduce the coupling losses in case of the fiber-to-silicon waveguide butt coupling configuration because of the better mode overlaps.

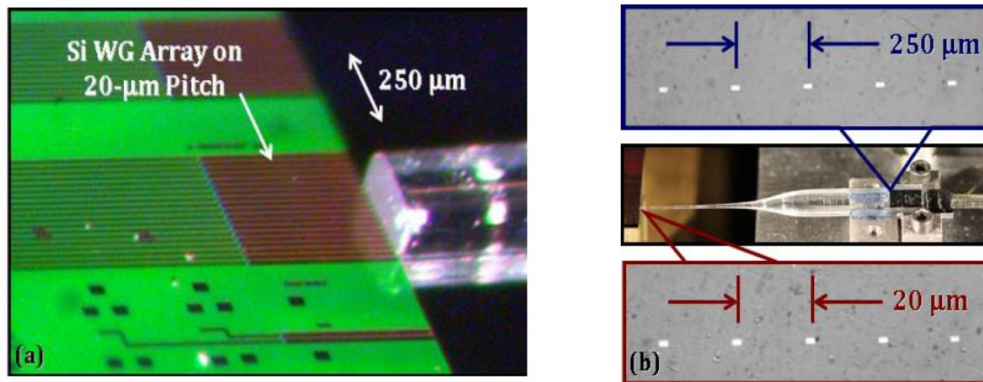

Figure 2.2 Fiber array which can be used to couple light in and out of the silicon plasmonic chips with channel pitch of 20 µm. (a) Optical microscope image of the but coupling configuration. (b) Scanning electron microscope images of the five channels at the wide-end and tapered-end of the pitch converter [1].

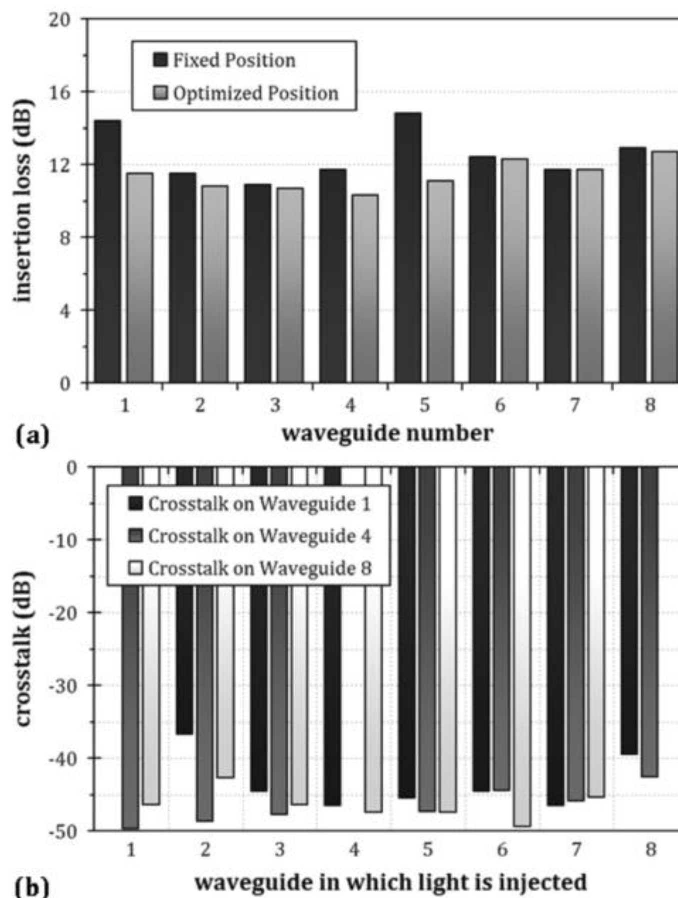

Figure 2.3 Plot of the (a) insertion loss and (b) cross talk of the 8 silicon waveguides coupled to the fiber array[1].

To characterize the coupling losses between the 8 channel silicon waveguide array with the fiber array channels, light is coupled to the all 8 silicon waveguide channels from the fiber array and the power transmission is measured at the other side of the waveguides using lensed fiber [1]. Figure 2.3 gives the insertion loss and the cross talk for all 8 channels [1]. An insertion loss of 9 dB has been reported for all 8 channels [1]. Approximately, 8.3 dB of the total insertion loss is attributed to the propagation losses in the silicon waveguide, to the pitch converter and to lensed fiber coupling. This results in less than 1 dB coupling losses between the 8 silicon waveguide and fiber array channels. Moreover, the observed cross talk among the channels is as small as -40 dB. Such a low cross talk in a 20 µm channel pitch is extremely difficult to achieve in the vertical stack packaging case, as we discuss later.

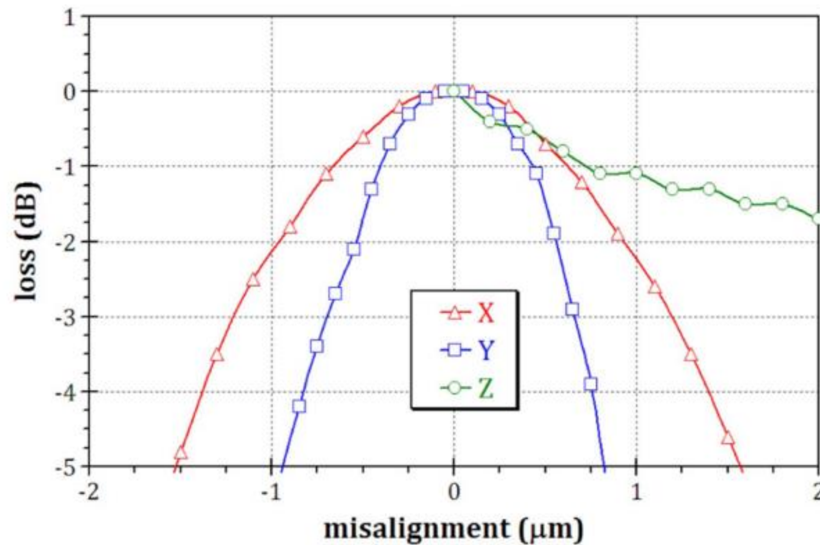

Figure 2.4 Normalized light coupling loss to the silicon waveguide as a function of the misalignment in all three coordinate axes [1]

Figure 2.4 gives the normalized coupling loss to the silicon waveguide as a function of the misalignment of the fiber array relative to its optimum position [1]. 1dB tolerances of ±0.7 µm, ±0.4 µm and ±0.7 µm is reported along the lateral (*X*), vertical (*Y*) and optical (*Z*) axes, respectively [1].

3 Vertical die stacking

Schematic of the 3D vertical packaging is given in Figure 3.1. First, the silicon-on-insulator chips with SiO_2 buried-oxide layer of 2 µm and the silicon device layer of 0.22 µm are processed for defining on-chip silicon-plasmonic transmitters and receivers. In the last fabrication step, the backside of one of the chips is etched to make the relative alignment possible in the flip chip stack configuration. Similar air hole is also made on the PCB carrier. Chips are mounted on the PCB board and the electrical bonding is performed.

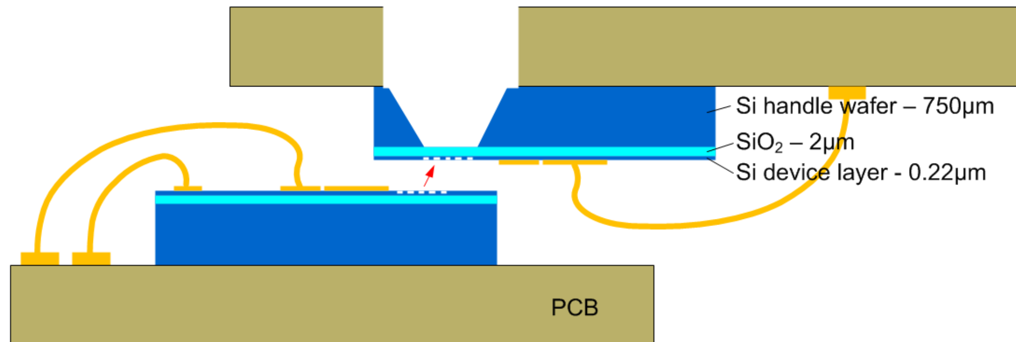

Figure 3.1 3D vertical stacking of electronic dies

Simple theoretically analysis is made to investigate the channel crosstalk, minimum acceptable channel pitch and optical losses. Assume the transmitter chip radiates Gaussian beam with the waist of 4, 8 …40µm (defined by the grating etch profile and size). The receiver chip which is located in a distance *d* away from the transmitter will receive a Gaussian field profile with the width of *w*, see Figure 3.2. The received Gaussian beam width *w* can analytically be calculated as a function of *d,* and is given in Figure 3.3.

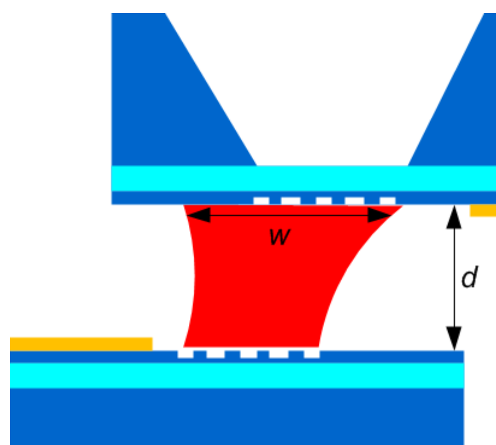

Figure 3.2 Schematic of the link comprising two grating couplers, and free-space communication channel. The transmitter chip (at the bottom) radiates the optical signal with a Gaussian beam profile into the free space. The receiver chip located in a distance *d* receives a Gaussian beam with the width of *w*.

As expected, the width of the received field profile increases with the increase of the distance *d* between the chips, see Figure 3.3. Based on the width of the received field profile, the minimum channel pitch resulting in an acceptable crosstalk is calculated as

$$\text{minimum pitch} = 2.5 \times w$$

Figure 3.4 gives the minimum channel pitch as a function of *d*. It can be seen that the target channel pitch of 50 μm can be achieved only with the chip-to-chip distances of below 100 μm.

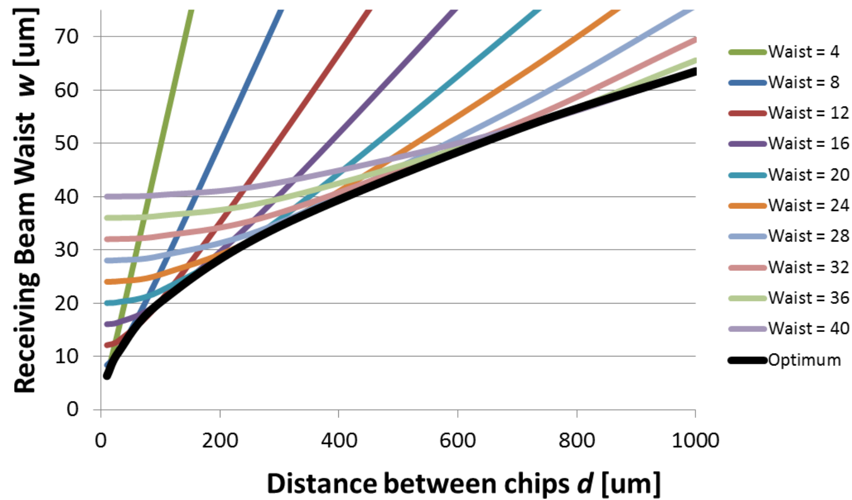

Figure 3.3 Receiving beam width *w* versus the chip-to-chip distance *d*.

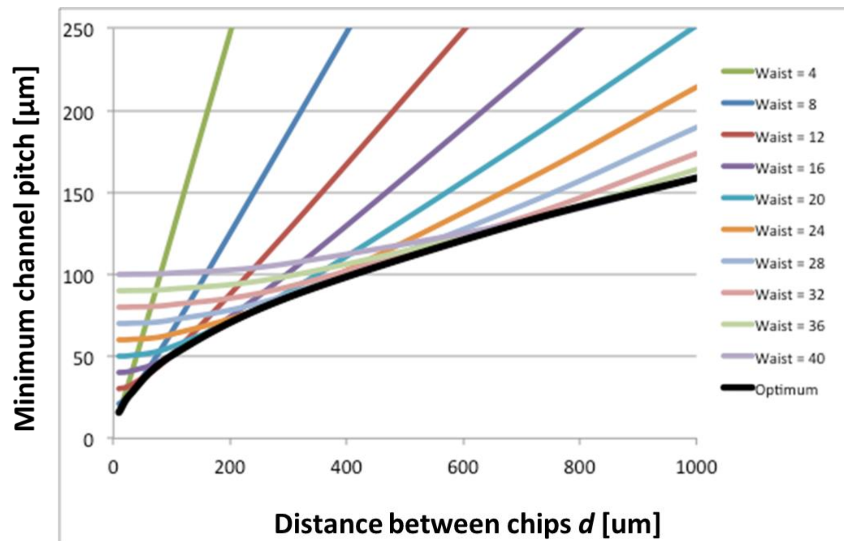

Figure 3.4 Minimum channel pitch as a function of the chip-to-chip separation *d*.

4 Comparison

Here we compare the two packaging scenarios for their performances and technological simplicities.

3D vertical stacking

Advantages

- Promising for realization of compact system-in-package systems.

Disadvantages

- Minimum achievable channel pitch is 50 µm.
- Less than 100 µm distance between the chips can make it difficult to maintain all the 8 modulators / detectors to PCB board electrical wires.
- The backside of one of the SOI chips should be etched. This means one more critical step is added to the entire fabrication process, which potentially can reduce the yield of the packaging.
- To overcome the high optical losses in plasmonic modulators or low power emission of plasmonic nanolaser, an optical preamplifier might be needed for the receiver. Vertical stack packaging does not allow an optical amplifier to be implemented in the system.
- The optical losses in the communication channel can be estimated to be around 8 dB(4 dB loss on each vertical grating coupler).

2D in-plane packaging

Advantages

- Achievable channel pitch is depended mainly on the fiber array. As discussed previously, fiber arrays with the channel pitch of less than 20 µm are available in the market.
- Very low cross talk level can be achieved even in the case of 20 µm channel pitch.
- No further fabrication steps are required.
- Allows large number of electrical wirings between the PCB boards and the SOI chips.
- An optical amplifier can be implemented in the link to improve the received signal quality.
- Using silicon inverted taper couplers, the optical losses in the channel can be kept within the limits of 2dB (1dB on each silicon taper-fiber array interface).

Disadvantage

- 2D packaging.
- Highly accurate alignment is required to align the fiber array to the silicon photonic chip.

Thus, the 2D in-plane packaging seems to be the most promising scenario for realizing NAVOLCHI's demonstrator.

5 References

1. F. E. Doany, B. G. Lee, S. Assefa, W. M. J. Green, M. Yang, C. L. Schow, C. V Jahnes, S. Zhang, J. Singer, V. I. Kopp, J. A. Kash, and Y. A. Vlasov, "Multichannel High-Bandwidth Coupling of Ultradense Silicon Photonic Waveguide Array to Standard-Pitch Fiber Array," IEEE J. Light. Technol. **29**(4), 475–482 (2011).