Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

M15 - Initial testing of bonded plasmonic lasers

Milestone no.:	M15
Due date:	01/10/2013
Actual Submission date:	07/02/2014
Authors:	Victor Calzadilla, TU/e Meint Smit, TU/e
Work package(s):	WP3
Distribution level:	RE[1] (NAVOLCHI Consortium)
Nature:	document, available online in the restricted area of the NAVOLCHI webpage

List of Partners concerned

Partner number	Partner name	Partner short name	Country	Date enter project	Date exit project
1	Karlsruher Institut für Technologie	KIT	Germany	M1	M36
2	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMCV	Belgium	M1	M36
3	TECHNISCHE UNIVERSITEIT EINDHOVEN	TU/e	Netherlands	M1	M36
4	RESEARCH AND EDUCATION LABORATORY IN INFORMATION TECHNOLOGIES	AIT	Greece	M1	M36
5	UNIVERSITAT DE VALENCIA	UVEG	Spain	M1	M36
6	STMICROELECTRONICS SRL	ST	Italy	M1	M36
7	UNIVERSITEIT GENT	UGent	Belgium	M1	M36

[1] **PU** = Public
PP = Restricted to other programme participants (including the Commission Services)
RE = Restricted to a group specified by the consortium (including the Commission Services)
CO = Confidential, only for members of the consortium (including the Commission Services)

Deliverable Responsible

Organization: Eindhoven University of Technology
Contact Person: Victor Calzadilla
Address: Faculty of Electrical Engineering
P.O. Box 513
5600 MB Eindhoven
The Netherlands
Phone: +31 (0) 40247 5129
E-mail: v.calzadilla@tue.nl

Executive Summary

This report describes the results of the first fabrication run of the laser devices, which was done according to the process flow presented in Deliverable 3.3. The main achievements and issues are discussed, as well as new ideas to improve the fabrication processing. Although lasing could not yet be demonstrated in this first run, it represents a significant progress towards the final demonstration of the metal-cavity nanolasers with waveguide coupling.

Change Records

Version	Date	Changes	Author
1 (submission)	07-02-14		V. Calzadilla, M. Smit

1. Introduction

The characterization of the first fabrication run of nanolasers on III-V samples bonded silicon is presented. All the important issues encountered during such first fabrication run, carried out following the process flow reported in Deliverable 3.3, are discussed in detail. While some of them are well understood, others remain a challenge that will require new ideas and further experiments to solve them before a nanolasers fabrication run is completely successful. Figure 1 shows the fabricated nanopillar laser cavity on an InP-membrane waveguide connected to a grating coupler.

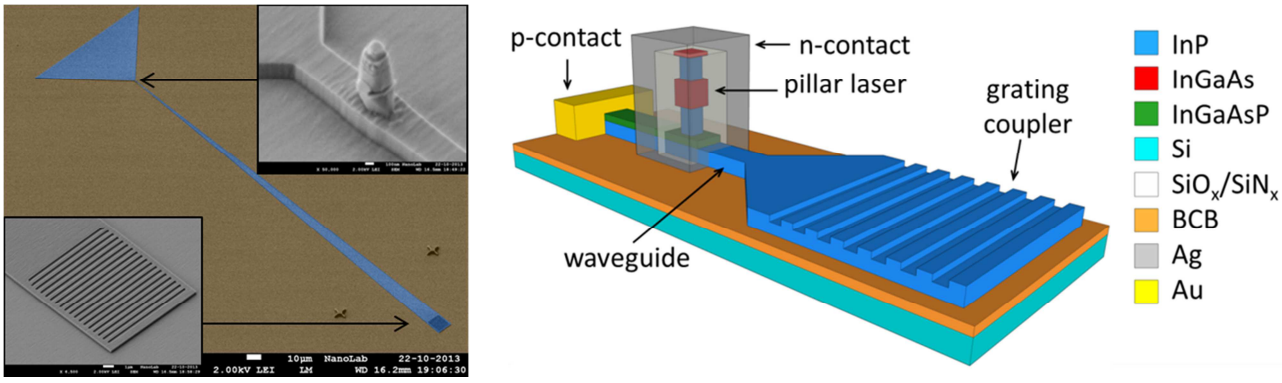

Figure 1. Left: Fabricated structure with artificial colour for easier comparison with the schematic at the right. Right: Schematic of the metal-cavity nanolaser.

In the next section of this report, the issues encountered during the first fabrication are presented and new ideas to solve them are discussed. It is worth highlighting that the fabrication results that are reported correspond to samples with the characteristics required for the device demonstrator, it means it is a bonded sample with a specific semiconductor layerstack and proper doping levels. Then, some conclusions are presented in the last section.

2. Characterization of first fabrication run

2.1. Non-vertical ICP etching of pillars

During the first electron-beam lithography (EBL), the pillars pattern is exposed using HSQ resist (negative tone). Then the pattern is transferred to the SiO_x beneath which acts as a hardmask to etch later the nanopillar with Inductively-Coupled Plasma Reactive-Ion Etching (ICP-RIE) using a CH_4-H_2 chemistry.

Although previous experiments (see Deliverable 3-3) demonstrated the possibility to achieve vertical etching and smooth sidewalls in the pillar, the pillars etched during the first fabrication run showed a sidewall angle of about 5° as shown in Fig 2. Such a large angle will result in a degradation of the cavity quality factor. This one and other cavity defects could lead to a laser source able to operate only at cryogenic temperatures.

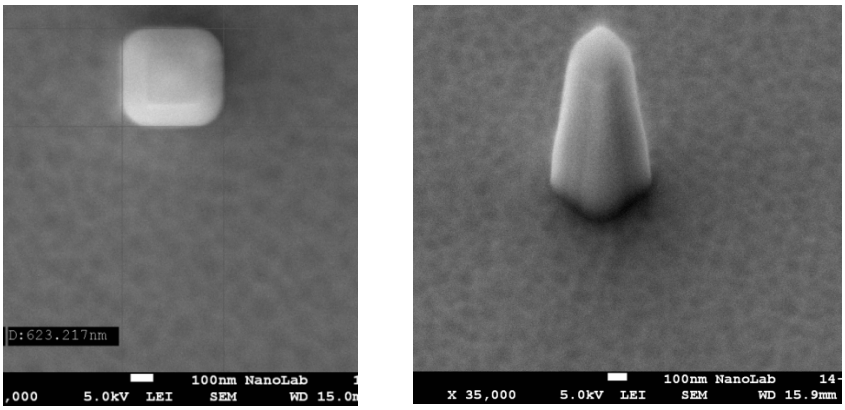

Figure 2. Left: Top view of the pillar showing that the pillar base is considerably wider than the top. Right: Etched pillar with the SiO_x hardmask on top.

The non-verticality of the pillars obtained in this bonded sample is thought to be due to a thermal problem. The BCB (Benzocyclobutene) layer used to perform the bonding of III-V to silicon, has a lower thermal conductivity than the one of the III-V semiconductors. Therefore, since such BCB is in between, it could limit the heat flow downwards leading to an overheating of the top of the sample. Then since our current ICP-RIE recipes at TU/e are tuned to provide a good result on pure III-V samples (non-bonded samples), we believe such over-heating causes non-optimum etching conditions.

In order to overcome this issue, we plan to optimize our ICP-RIE etching recipe to properly etch nanostructures in III-V samples bonded to silicon. The first ideas point to use a low temperature recipe or a lower RF bias in order not to overheat the sample, however detailed etching tests are required to find out an optimum recipe.

2.2. Mask erosion of pillar protection

The fabrication of the grating coupler is done after the pillars and waveguides have been etched. During their etching, the original pillar hardmask (SiO_x) and the hardmask to etch the waveguides (HSQ) are preserved to prevent the etching of these structures. Figure 3(left) shows the pillar and waveguide protected by the hardmasks.

Nevertheless, during the etching of the gratings hardmask (Si_xN_x/HSQ), the pillar hardmask was eroded in a way that the top of the pillars resulted unprotected. Therefore, during the semiconductor etch of the gratings, the top of pillars was also (unintentionally) etched as can be observed in Fig 3(right).

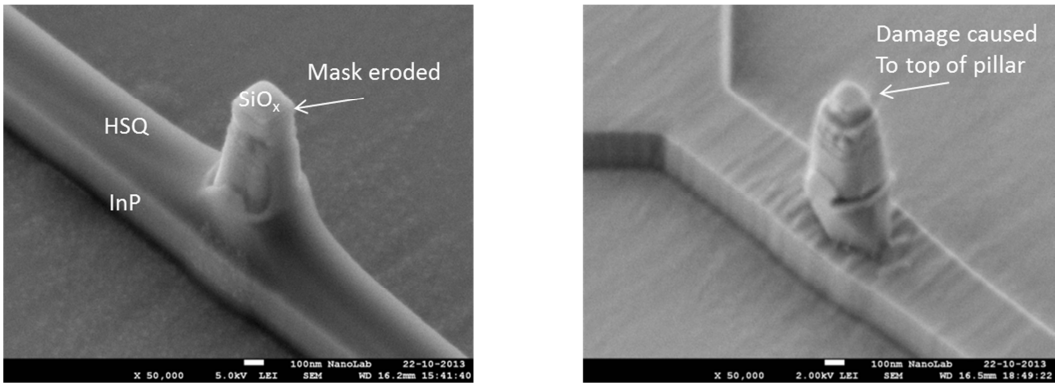

Figure 3. Left: Pillar on waveguide, both structures are protected by their original hardmasks. Right: Structure after gratings etching and hardmasks removal. The top of the pillar is visibly damaged.

In further fabrication runs, an additional lithography step will be included to completely protect the pillars with a thick photoresist layer.

2.3. Low quality of SiO_x

After the semiconductor nanostructures were fabricated (i.e. pillar, waveguide and grating coupler), a 175 nm thick layer of SiO_x layer is deposited to function as electrical insulation layer and also to minimize the metal loss in the laser cavity. Figure 4 shows a typical structure after the SiO_x has been deposited by plasma-enhances chemical vapor deposition (PECVD). As can be seen, the SiO_x is quite rough, it consists of grains rather than being a homogeneous material.

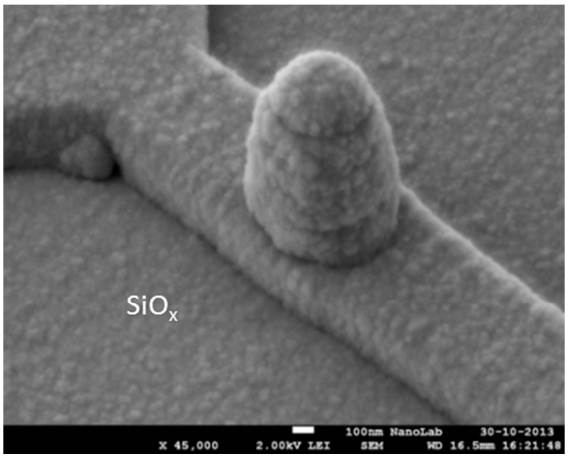

Figure 4. Pillar on waveguide with SiOx deposited on top by PECVD.

The optimization of the PECVD recipe to get a more smooth SiO_x has started. Current results are promising (shown in Fig. 5), but additional effort is still required to get an optimum recipe to deposit a smooth SiO_x that preferably does have the same deposition rate in both horizontal and vertical surfaces.

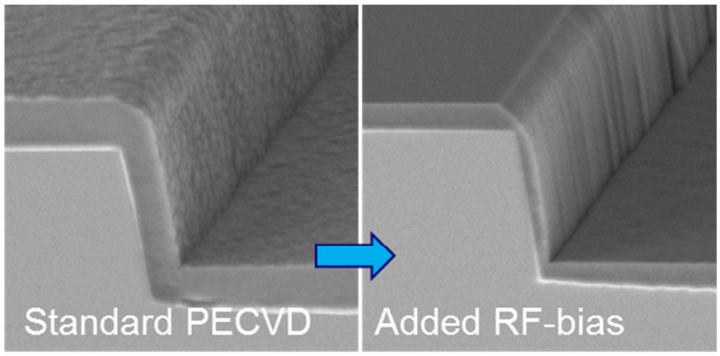

Figure 5. Left: InP ridge with a SiO_x cladding deposited with the typical recipe in TU/e cleanroom. Right: Ridge with a smoother SiO_x cladding achieved by lowering the RF bias. The deposition rate on the top is about twice the sidewall deposition rate.

2.4. Outgasing during annealing

The annealing of silver at 400 °C was found to be required to increase the silver grain size, and therefore improve the material quality, as described in Deliverable 3.3. The silver homogeneity is important because it will ultimately influence the cavity quality factor through absorption and scattering loss.

As can be seen in Fig. 6, the rapid thermal annealing caused round defects with sizes of a few hundred micrometers. Since the defects have a round shape, they could corresponds to outgassing of some material in the sample, which most likely is BCB since its decomposition temperature is 350 °C as reported by the supplier.

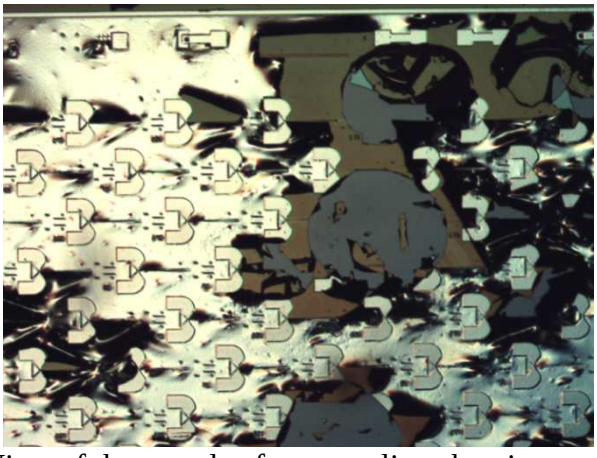

Figure 6. View of the sample after annealing showing round defects.

In order not to get outgassing, the annealing will be done at lower temperatures in further processing runs. Nevertheless, since silver is not optimally annealed at lower temperatures, detailed experiments are required to determine which annealing temperature does not compromise considerably the silver quality in bonded samples.

2.5. Non-etching of silver

After silver and gold have been deposited by thermal evaporation, the full wafer is covered by metal and therefore all the devices are electrically connected. For such reason, the metal has to be etched in some regions to isolate the devices. This is done by protecting the devices (typically only the laser cavity and the n-contact area are protected) with photoresist and then wet etching the silver everywhere else. Figure 7 shows an example of the device protected by photoresist.

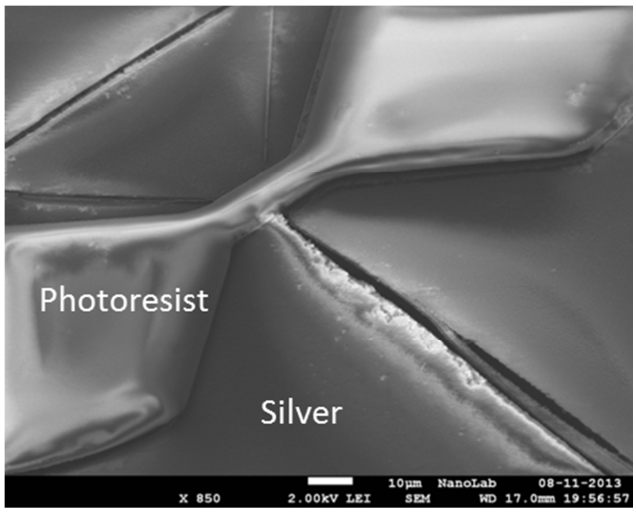

Figure 7. Device covered with photoresist to protect it during the silver etching.

In principle, the etching of silver and gold can be done with a KCN-based etchant, nevertheless it was not possible to completely etch these metals during the current fabrication. It was found that only non-annealed silver was etched, whereas the silver layer that was annealed was not etched at all. As this problem is not well understood yet, additional experiments are required with the same etchant and other alternatives as well.

3. Conclusions

The main results of the first fabrication run have been described in this report. Due to the unexpected issues described above, the first fabrication run of the laser devices was not fully succesfull. Despite the current technological issues, the fabrication of these nanolasers is promising and we expect to achieve laser operation in the coming months.