Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Data Codecs for Power Consumption Reduction

Milestone no.:	M29
Due date:	01/31/2013
Actual Submission date:	04/05/2013
Authors:	ST
Work package(s):	WP5
Distribution level:	RE[1] (NAVOLCHI Consortium)
Nature:	document, available online in the restricted area of the NAVOLCHI webpage

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Executive Summary

This document describes algorithms and implementations related to encoders and corresponding decoders aiming at reducing the switching activity over transmission channels in order to minimize the dynamic power consumption. The outcome of some studies about encoding techniques for error detection and correction is reported as well.

Change Records

Version	Date	Changes	Author
0.1 (draft)	2013-02-11	First version	Alberto Scandurra
1 (submission)	2013-04-05	Final version	Alberto Scandurra

Contents

1. Introduction

Power consumption is a critical factor in modern electronics.
Nowadays, long duration of batteries is an essential requirement for any consumer good, while environment-aware technology and energy saving have become widespread matters of concern for the industry.

Power consumption in electronic systems depends on many variables, such as the specific data patterns they elaborate, the overall architecture, the specific implementation of some modules, the speed (in the terms of clock frequency). Improving power performance of a system involves the whole design.

As far as communication systems are concerned, single on-chip and off-chip links and complete NoCs (Networks on Chip) and NiPs (Networks in Package) can be responsible of a large percentage of the total power consumption. Encoding transmission techniques can achieve relevant advantages in this sense, and are then regarded with interest both in industrial and scientific fields. These techniques aim to transform (code) the information, so that less power consumption is required. They include data-format compression at the topmost software level, architectural choices and specific modules in hardware.

2. Encoding techniques to reduce power consumption

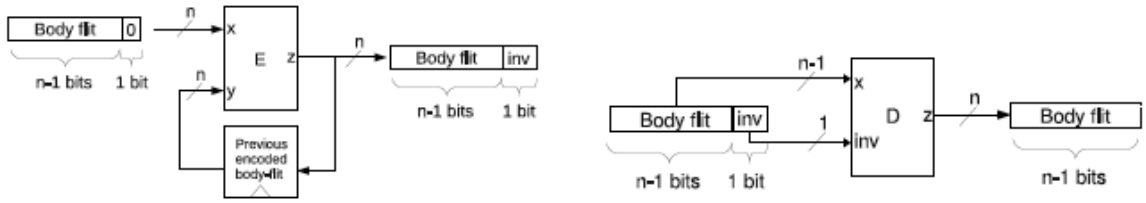
This chapter presents a set of techniques and the results in terms of power-saving they can achieve on SoCs (Systems on Chip) and SiPs (Systems in Package) links and on end-to-end NoC/NiP communication.

The presented techniques are:

- Bus Inverter (BI)
- A variant of Bus Inverter by University of Catania (UniCT BI)
- Half-Identity Half-Reverse Transition Signaling (HIHRTS)
- XOR-based Probability Redistribution (XOR PR)

1. Bus Inverter

This technique simply consists of a conditional inversion of bits in input: given a bus of N bit as input, current value of each bit is compared with its previous value to determine whether a transition is expected.
When the number of transitions in a phyt (which means the *Hamming distance* between the current phyt and the previous one) exceeds half the bus size, then the entire bus is inverted (because the inverted bus will have minor Hamming distance to the previous phyt).
To inform the decoder whether or nor the bus has been inverted, an additional flag line is required.



Apart from introducing area overhead for the additional line, this scheme is recognized to be *general purpose*, but not very efficient, except for random data patterns (mutually independent phyts) and extreme study cases.
Moreover, RTL basic implementations' performance is not very impressive in terms of area, time and scalability: adders/counters required to determine the inversion condition are slower and lower while the bus size increases.

A segmented approach, which means a selective inversion of sections of the input bus, has been implemented as well, accepting additional flag lines. Such parallel version of Bus Inverter provides far better performance than the single-block counterpart, as shown below.

Bus Inverter is a patent of AST group of STMicroelectronics™.

2. Bus Inverter variant from University of Catania

As an enhancement of Bus Inverter, the inversion condition is not triggered according to

Hamming distance, but takes into account a *dynamic power model applied to the bus lines*[6][7] developed by Univerity of Catania.
According to a 2-bit granular algorithm, dynamic power model of the bus lines is used to determine whether or not it is convenient to invert the flit.

Power model proposed[6][7] for CMOS dynamic power is:

$$P = [T_{0\to1}(C_S + C_l) + T_C C_C]V_{dd}^2 F_{ck}$$

where V_{dd} is the supply voltage, F_{ck} is clock frequency, C_S is the self capacitance (including parallel plate and fringe capacitance) and C_l is the load capacitance.
$T_{0\to1}$ and T_C are the average number of effective transitions per cycle associated with C_S and C_C respectively.

T_C can then be expressed as a weighted addition of the transition types:

Time	Normal			
	Type I			
$t-1$	00	00	11	11
t	01	10	01	10
	Type II			
$t-1$	01	10		
t	10	01		
	Type III			
$t-1$	00	11		
t	11	00		
	Type IV			
$t-1$	00	11	01	10
t	00	11	01	10
	T_4^*		T_4^{**}	

$$T_C = k_1 T_1 + k_2 T_2 + k_3 T_3 + k_4 T_4$$

Some literary works[6][7][18] have determined:

$$k_1 = 1 k_2 = 2 k_3 = k_4 = 0$$

so that, being the effective capacitance of Type II transitions usually twice that of Type I transitions, power model can be reformulated as:

$$P = [T_{0\to1}(C_S + C_l) + (T_1 + 2T_2)C_C]V_{dd}^2 F_{ck}$$

It is clear that power-saving can be achieved by minimizing the number of Type I and Type II transitions and global $T_{0\to1}$.

The encoding scheme must then compute whether or not it is convenient to invert in terms not only of switching activity, but also of effective capacitance.
Operation performed takes into account power consumption in both cases (non-inverted phyt and inverted phyt).

$$P \propto T_{0\to1}C_S + (k_1T_1 + k_2T_2 + k_3T_3 + k_4T_4)C_C$$
$$P' \propto T'_{0\to1}C_S + (k_1T'_1 + k_2T'_2 + k_3T'_3 + k_4T'_4)C_C$$

The phyt is then inverted when P' < P, which means that the inverted phyt requires less power consumption.
$T'_{0\to1}$ equates $T_{0\to0}$ while T'_1, T'_2, T'_3 and T'_4 can be reformulated with correspondance to T_1, T_2, T_3 and T_4 from the scheme below:

Time	Normal				Inverted			
	Type I				Type I			
$t-1$	00	00	11	11	00	00	11	11
t	01	10	01	10	10	01	10	01
	Type II				Type IV			
$t-1$	01	10			01	10		
t	10	01			01	10		
	Type III				Type IV			
$t-1$	00	11			00	11		
t	11	00			00	11		
	Type IV				Type II and III			
$t-1$	00	11	01	10	00	11	01	10
t	00	11	01	10	11	00	10	01
	T_4^*		T_4^{**}		T_3		T_2	

$$P' \propto T_{0\to0}C_S + [k_1T_1 + K_2T_4 + k_3T_4 + k_4(T_2 + T_3)]C_C$$

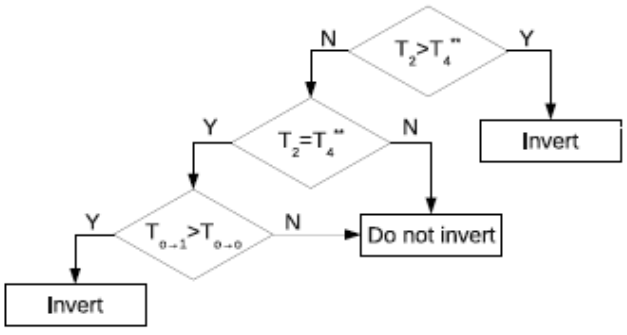
Assuming[6][7][18]

$$k_1 = 1k_2 = 2k_3 = k_4 = 0C_C/C_S = 4$$

invert condition P' < P is equalent to

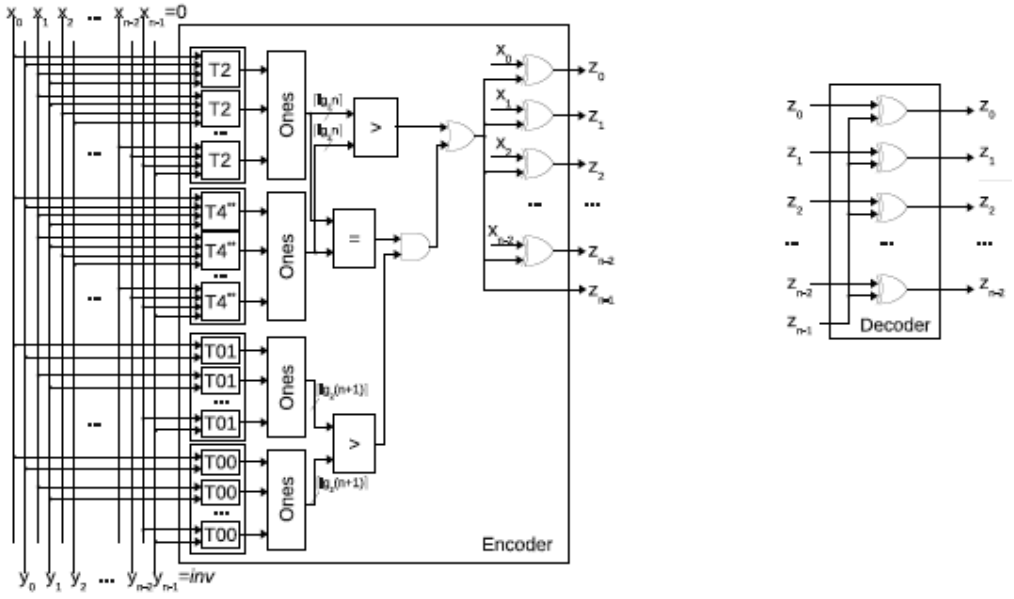
$$T_{0\to1} + \delta T_2 > T_{0\to0} + \delta T_4$$

Encoder algorithm is then:



While decoder module is exactly the same as the previous technique, encoder module stores the

previously transmitted flit and compares it with the following one, in order to determine not only how many transitions are expected, but also the type of these.



Encoder and decoder schemes

Required logic can be lighter than the one of Bus Inverter, but still remarkable for area and critical path. Higher speed is expected, as well as better power consumption savings. Segmented approaches can be pursued similarly to Bus Inverter.

3. Half-Identity Half-Reverse Transition Signaling

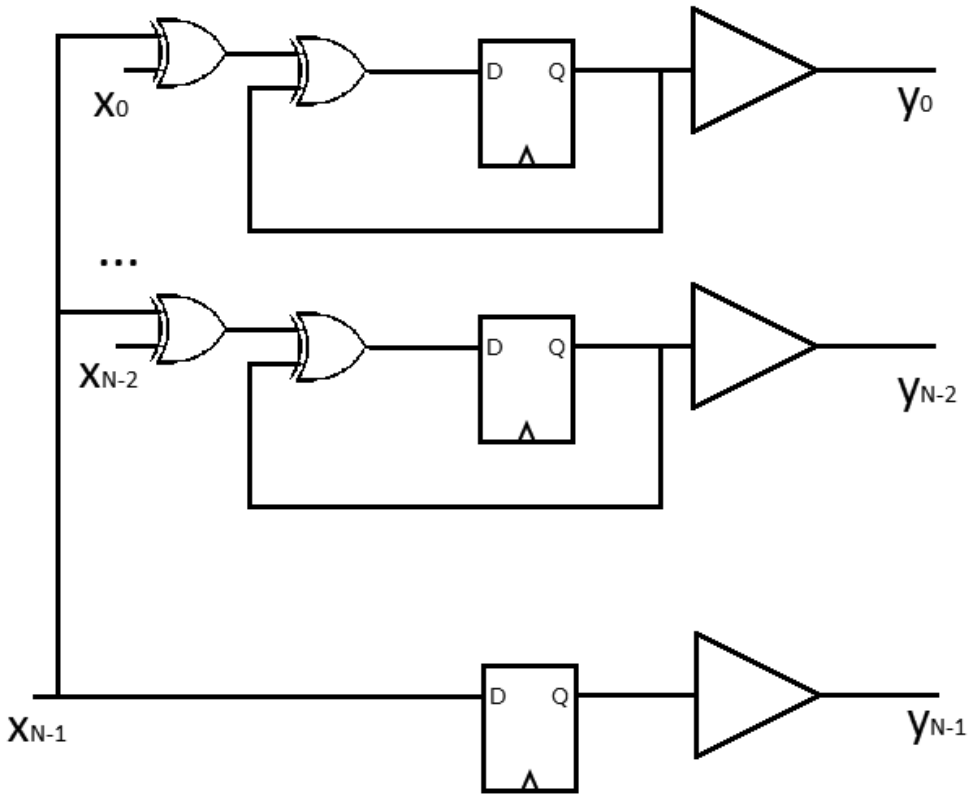
This technique does not invert bits, but relies on *information coding to reduce transitions*. No redundancy lines are required.

A relatively simple, fast and granular coding logic reduces overhead of power and area, while no flag lines are required, making HIHRTS a more efficient technique in high frequency applications.
The encoder executes *XOR* operation between the input bus and the most significant bit (and then each bit of the bus is inverted if MSB value is 1) and the result of such operation is XOR-ed again to the previously transmitted phyt. Resulting logic consists of only two sequential XOR ports and one flip flop per bit (to store the previous phyt).

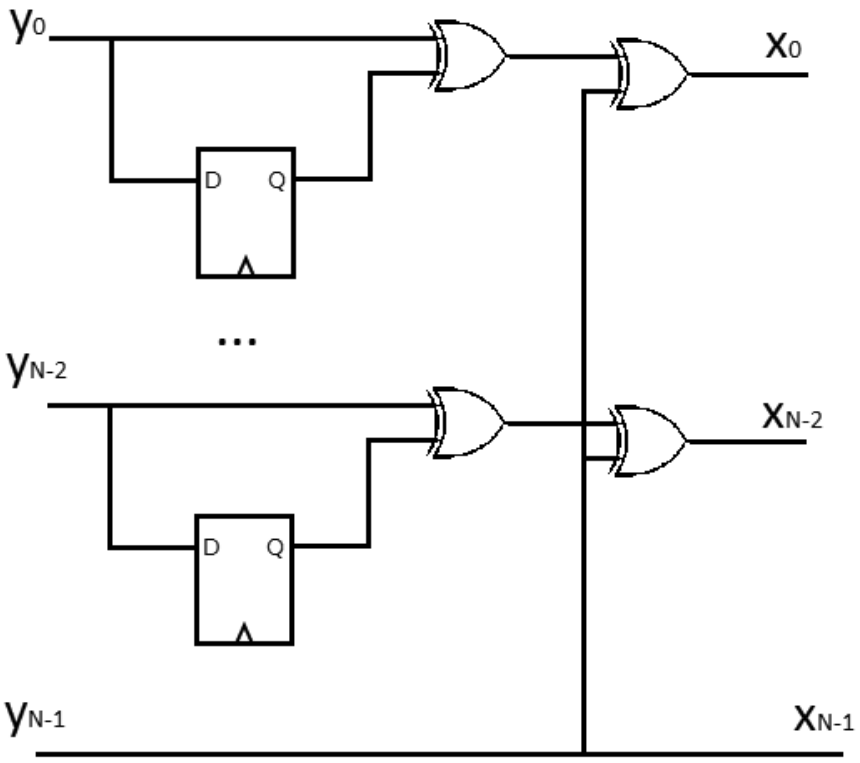
The decoder executes reverse operation, as the algorithm sets the MSB (which is not altered in any way) as a decoding key to reconstruct the original phyt (XOR's inverse operation is XOR itself, so the decoder is as simple as the encoder).

Moreover HIHRTS' performance is expected to be worse than Bus Inverter with random traces and in extreme study cases. Anyway it behaves far better when the occurrence of ones (or zeros)

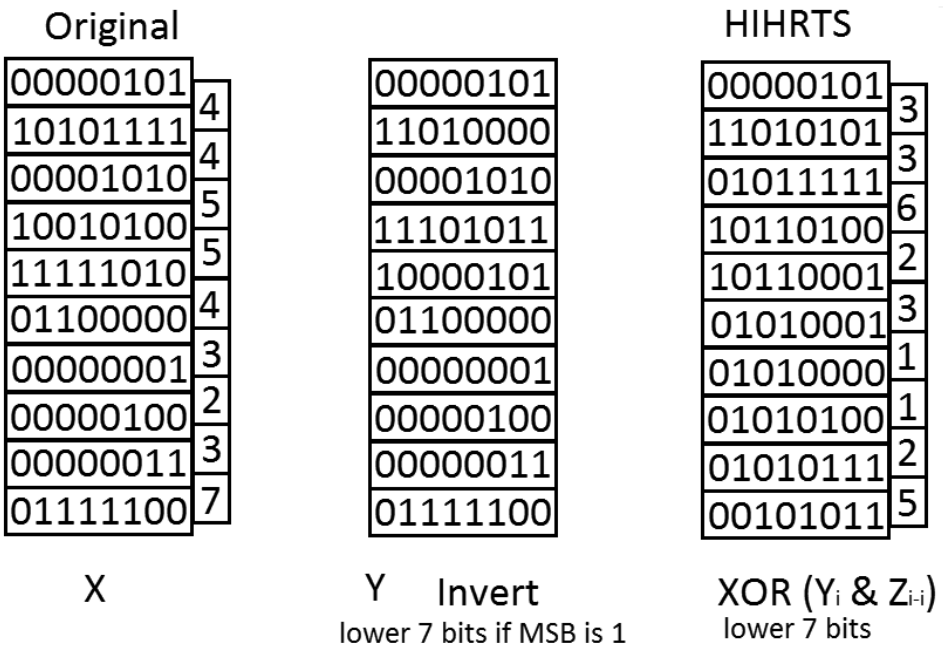
dominates input bus in highly-transient, but still realistic, patterns.



Encoder Scheme



Decoder scheme



HIHRTS is a proposal from indian OCCS group of STMicroelectronics™.

4. XOR-based redistribution of probability

This technique is designed for non-compressed videos. It does not *explicitly* make use of the previous phyt to determine the encoded phyt.

During the encoding phase, current input phyt is divided into pairs, with strict 2-bit granularity. For each pair, one bit remains uncoded while the other is processed as the XOR of the pair. Decoding phase is symmetrical (XOR inverts itself).

Considering the succession of phyts, this technique relies on a redistribution of probability: considering the pair, when double inversions are less probable than single inversions, switching activity is statistically reduced.

PREV NE	PREV E	CURR NE				CURR E			
0 0	0 0	0 0 **0**	0 1 **1**	1 0 **1**	1 1 **2**	0 0 **0**	1 1 **2**	1 0 **1**	0 1 **1**
0 1	1 1	0 0 **1**	0 1 **0**	1 0 **2**	1 1 **1**	0 0 **2**	1 1 **0**	1 0 **1**	0 1 **1**
1 0	1 0	0 0 **1**	0 1 **2**	1 0 **0**	1 1 **1**	0 0 **1**	1 1 **1**	1 0 **0**	0 1 **2**
1 1	0 1	0 0 **2**	0 1 **1**	1 0 **1**	1 1 **0**	0 0 **1**	1 1 **1**	1 0 **2**	0 1 **0**

Max Probability

Medium Probability

Minimum Probability

PROBABILITY MATRIX (%)			
30	6	3	5
6	6	5	1
3	5	5	1
5	1	1	11

SR	**31**
SRE	**28**

highway_cif.yuv			
12	3	3	5
3	13	4	2
3	4	10	3
5	2	3	18

SR	**29**
SRE	**26**

mb.dat			
30	6	3	5
6	6	5	1
3	5	5	1
5	1	1	11

SR	**31**
SRE	**28**

hd.mp4			
6	6	6	6
6	6	6	6
6	6	6	6
6	6	6	6

SR	**48**
SRE	**48**

container_cif.yuv			
11	3	2	4
3	15	5	2
2	5	14	3
4	2	3	13

SR	**28**
SRE	**25**

XOR PR is a proposal by Daniele Mangano of OCCS group of STMicroelectronics™.

2. Speed and scalability issues

As anticipated above, speed and scalability are critical issues for both Bus Inverter and its UniCT variant version. Their 72-bit static CMOS implementations offer maximum clock limit, in synchronous mode, around 300 – 400 MHz, depending on the technology.

The main cause for this issue is the need for big (and slow) counters (or adders). These components' performance strongly depends on the bus size, which is the number of bits processed.

$$t_{delay} = Nt_{carry} + t_{\Sigma}RippleCarryAdder$$

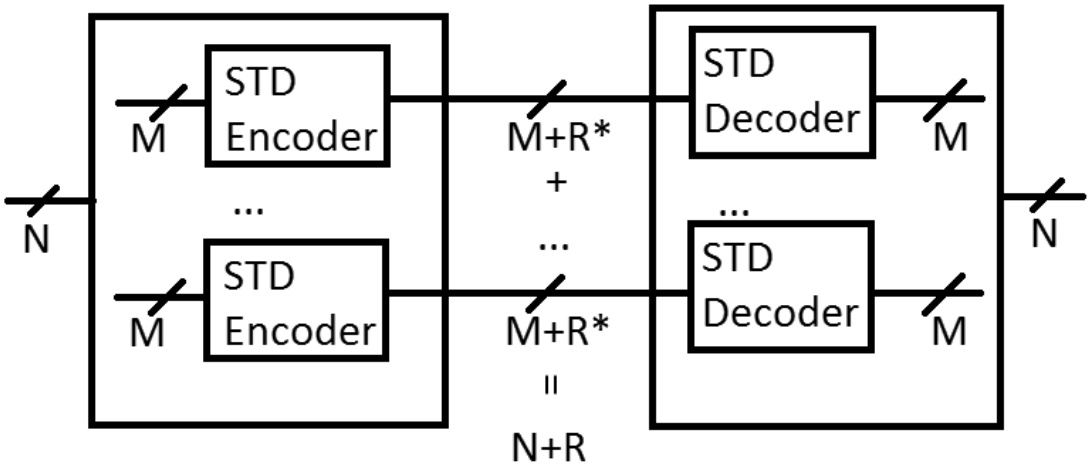
$$t_{delay} = t_{setup} + (2M-1)t_{carry} + (\frac{N}{M}-1)t_{MUX} + t_{\Sigma}CarryBypassAdder(MMUX)$$

$$t_{delay} = t_{setup} + Mt_{carry} + \frac{N}{M}t_{MUX} + t_{\Sigma}LinearCarrySelectAdder(MMUX)$$

$$t_{delay} = t_{setup} + (\frac{\alpha}{2} + \sqrt{2\alpha N})t_{carry} + t_{\Sigma}SquareRootCarrySelectAdder(t_{MUX} \sim \alpha t_{carry})$$

Different adders show different propagation delay dependence on number of bits N.

An improvement to such limits can be obtain through segmented coding algorithms: encoding technique is performed on a smaller set of bits, so that the whole encoder is divided into a group of fast modules, which operate in a parallel mode.



Segmentation scheme

It is important to highlight that a segmented algorithm is different from the original one: different results are expected not only in terms of speed, but also for the final switching activity reduction.

Subsequently, the decoder must be segmented as well.

Byte-size standard modules have been implemented and tested with regard to their single-block counterpart.
Standard modules are faster, because each of them has smaller bus size, and operate in parallel, regardless of their number. This provides scalability to the whole system and higher working frequencies (500 – 700 MHz), at the cost of further redundancy lines (one per module).

Segmented HIHRTS was synthesized too, but speed improvement is far less significant, because the MSB fan-out is the only difference, in terms of load capacitance, between the two versions.
This module was already more scalable and fast than BI and UniCT BI.
Anyway the algorithm changes, as multiple decoding keys are used, so that switching activity reduction is different.

As far as XOR Redistribution of Probability is concerned, a segmented version is not possible, as the algorithm is already fully parallel, with 2-bit strict granularity.

3. Synthesis data

Following data describe the implemented techniques, making use of libraries from 65 nm static CMOS technologies on 0.5 pF load.

Project	Clock limit*	Power overhead**	Area overhead	Redundancy
Bus Invert (72-bit single-block)	300 MHz	2.46 + 0.82 mW	4225 + 439 standard cells	1 flag line
Bus Invert (8-bit segmented)	550 MHz	2.81 + 0.81 mW	5856 + 1555 standard cells	9 flag lines
hihrTS (72-bit single-block)	933 MHz	6.17 + 2.27 mW	3536 + 2755 standard cells	No redundancy
hihrTS (8-bit segmented)	1000 MHz	5.75 + 2.36 mW	2837 + 2709 standard cells	No redundancy
XOR PR (72-bit single-block)	1033 MHz	3.5 + 1.3 mW	1857 + 1326 standard cells	No redundancy

Following data describe the implemented techniques, making use of libraries from *40 nm static CMOS technologies* on 0.5 pF load.

Project	Clock limit*	Power overhead**	Area overhead	Redundancy
Bus Invert (72-bit single-block)	350 MHz	2.51 + 0.28 mW	3654 + 182 standard cells	1 flag line
Bus Invert (8-bit segmented)	600 MHz	2.18 + 0.63 mW	3451 + 912 standard cells	9 flag lines
hihrTS (72-bit single-block)	1000 MHz	5.62 + 1.79 mW	2838 + 2135 standard cells	No redundancy
hihrTS (8-bit segmented)	1000 MHz	5.15 + 1.53 mW	2490 + 1633 standard cells	No redundancy
XOR PR (72-bit single-block)	1033 MHz	3 + 0.92 mW	1338 + 694 standard cells	No redundancy

Following data are obtained with libraries from *32 nm static CMOS technologies* on 0.5 pF load.

Project	Clock limit*	Power overhead**	Area overhead	Redundancy
Bus Invert (72-bit single-block)	375 MHz	1.67 + 0.23 mW	1015 + 129 standard cells	1 flag line
Bus Invert (8-bit segmented)	700 MHz	1.83 + 0.62 mW	1473 + 562 standard cells	9 flag lines
hihrTS (72-bit single-block)	1167 MHz	4.39 + 1.59 mW	825 + 955 standard cells	No redundancy
hihrTS (8-bit segmented)	1167 MHz	4.13 + 1.46 mW	808 + 871 standard cells	No redundancy
XOR PR (72-bit single-block)	1200 MHz	2.55 + 0.87 mW	613 + 399 standard cells	No redundancy

* assuming input delay = 15% clock period, output delay = 10% clock period
** comprehensive of dynamic and static power consumption at the maximum working frequency (thus values are not directly comparable)

4. Switching activity analysis

According to the dynamic power model of bus lines

$$P_{dyn} = \alpha C_L V_{swing}^2 f_{ck}$$

dynamic power depends linearly on the line switching activity α, which is the probability of a commutation for each line. Evaluation of switching activity can be performed through Laplace definition, as the number of occurrences divided for the total bit number.

Collected data confirm Bus Inverter to be generically valid, but its effectiveness may dramatically differ from case to case, as shown.

It can be noted than HIHRTS tends to flatten switching activity from almost every value (high or low as it may be) to an average 0.3 – 0.5 switching activity, with best results with highly-transient traces. A minor variant of HIHRTS, named Double Keying HIHRTS, consisting of another XOR port added to the logic and another bit used as decoding key, statistically performs worse than the single keying counterpart. It is shown only for comparison.

It is important to observe that as far as University of Catania variant technique is concerned, this model is inadequate to evaluate the effective reduction in power consumption, because this technique also considers the capacitance. Collected data are therefore scarcely relevant in regard of this technique. Better characterizations for such variant would be obtained evaluating the product αC_L.

Note that the following *data do not take into account redundancy lines* (if present).

Random input (72 bits)	Reference: α = 0.356	Improvement
Bus Invert (72-bit single-block)	α = 0.349	-1.95%
UniCT Bus Invert (72-bit single-block)	α = 0.496	+39.45%
hihrTS (72-bit single-block)	α = 0.467	+31.25%
Double keying hihrTS (72-bit single-block)	α = 0.503	+41.2%

It is here shown how uncorrelated (random generated) input strings determine bad performance for all the cited techniques. Improvement provided by Bus Inverter for random bits is weak and realistically not worth the area and power cost of the components.

Gray code input (72 bits)	Reference: α = 0.014	Improvement
Bus Invert (72-bit single-block)	α = 0.014	0.00%
UniCT Bus Invert (72-bit single-block)	α = 0.014	0.00%
hihrTS (72-bit single-block)	α = 0.036	+157.14%
Double keying hihrTS (72-bit single-block)	α = 0.035	+148.0%

Inputs with strong preexisting coding provide similar effects, as none of the module manages to improve the switching activity further: Bus Inverter determines no advantage in inverting the bus, and thus leaves the input unchanged, while additional coding from HIHRTS even worsen the switching activity.

Fully-transient input (72 bits)	**Reference: α = 1**	**Improvement**
Bus Invert (72-bit single-block)	α = 0.0	negative infinite
UniCT Bus Invert (72-bit single-block)	α = 1	0.00%
hihrTS (72-bit single-block)	α = 0.0140	-98.61%
Double keying hihrTS (72-bit single-block)	α = 0.514	-48.6%

Another extreme study case regards sequences of strings in which every bit is continuously changed. This situation is the ideal case for Bus Inverter, as it manages to nullify the number of transitions. HIHRTS is also very effective, as it implicitly transforms the entire sequence into a Gray code (almost single transition per string).

16-bit block-transient traffic	**Reference: α = 0.525**	**Improvement**
Bus Invert (72-bit single-block)	α = 0.4	-23.81%
UniCT Bus Invert (72-bit single-block)	α = 0.525	0.00%
hihrTS (72-bit single-block)	α = 0.447	-14.81%
Bus Invert (8-bit composed system)	α = 0.190	-36.11%
hihrTS (8-bit composed system)	α = 0.25	-52.38%
Double keying hihrTS (72-bit single-block)	α = 0.463	-11.78%

This scheme makes use of sequences of binary strings where groups of 16 adjacent bits are changed together. What is obtained is an average input switching activity, making the case more realistic. Segmented Bus Inverter shows more effective than the single-block counterpart: every standard module can exploit the characteristics of the string segment and choose whether or not to invert the line. HIHRTS shows very effective, especially the modular version.

8-bit block-transient traffic	Reference: α = 0.511	Improvement
Bus Invert (72-bit single-block)	α = 0.43	-15.85%
UniCT Bus Invert (72-bit single-block)	α = 0.511	0.00%
hihrTS (72-bit single-block)	α = 0.45	-11.94%
Bus Invert (8-bit composed system)	α = 0.23	-54.99%
hihrTS (8-bit composed system)	α = 0.40	-21.72%
Double keying hihrTS (72-bit single-block)	α = 0.44	-13.84%

This scheme is similar to the previous one, and results shown are consistent with what previously observed for average input switching activities. It confirms that better performance can be achieved through segmented versions when the traces present some spatial locality.

Highly-transient traffic	Reference: α = 0.752	Improvement
Bus Invert (72-bit single-block)	α = 0.247	-67.15%
UniCT Bus Invert (72-bit single-block)	α = 0.752	0.00%
hihrTS (72-bit single-block)	α = 0.172	-77.13%
Bus Invert (8-bit composed system)	α = 0.180	-76,00%
hihrTS (8-bit composed system)	α = 0.217	-71.14%
Double keying hihrTS (72-bit single-block)	α = 0.535	-28.80%

With high switching activity as input, all the techniques perform efficiently.

Application-oriented analysis for the indicated data types performed on the testbench as follows:

MP3 music files	**Reference: α = 0.492**	**Improvement**
Bus Invert (72-bit single-block)	α = 0.448	-8.94%
hihrTS (72-bit single-block)	α = 0.488	-0.81%
Bus Invert (8-bit composed system)	α = 0.361	-26.63%
hihrTS (8-bit composed system)	α = 0.486	-1.22%
XOR PR (72-bit single-block)	α = 0.493	+0.20%

PDF text files	**Reference: α = 0.464**	**Improvement**
Bus Invert (72-bit single-block)	α = 0.429	-7.54%
hihrTS (72-bit single-block)	α = 0.478	+3.02%
Bus Invert (8-bit composed system)	α = 0.352	-24.14%
hihrTS (8-bit composed system)	α = 0.480	+3.45%
XOR PR (72-bit single-block)	α = 0.481	+3.66%

JPG picture files	**Reference: α = 0.488**	**Improvement**
Bus Invert (72-bit single-block)	α = 0.444	-9.02%
hihrTS (72-bit single-block)	α = 0.491	+0.61%
Bus Invert (8-bit composed system)	α = 0.359	-26.43%
hihrTS (8-bit composed system)	α = 0.492	+0.82%
XOR PR (72-bit single-block)	α = 0.489	+0.20%

TXT text files	Reference: α = 0.327	Improvement
Bus Invert (72-bit single-block)	α = 0.327	0.00%
hihrTS (72-bit single-block)	α = 0.478	+46.18%
Bus Invert (8-bit composed system)	α = 0.310	-5.20%
hihrTS (8-bit composed system)	α = 0.478	+46.18%
XOR PR (72-bit single-block)	α = 0.403	+23.24%

WMV video files	Reference: α = 0.488	Improvement
Bus Invert (72-bit single-block)	α = 0.445	-8.81%
hihrTS (72-bit single-block)	α = 0.485	-0,61%
Bus Invert (8-bit composed system)	α = 0.358	-26.64%
hihrTS (8-bit composed system)	α = 0.481	-1.43%
XOR PR (72-bit single-block)	α = 0.490	+0.41%

YUV-CIF video files	Reference: α = 0.291	Improvement
Bus Invert (72-bit single-block)	α = 0.281	-3.44%
hihrTS (72-bit single-block)	α = 0.510	+75.26%
Bus Invert (8-bit composed system)	α = 0.233	-19.93%
hihrTS (8-bit composed system)	α = 0.552	+89.69%
XOR PR (72-bit single-block)	α = 0.281	-3.44%

YUV-QCIF video files	Reference: α = 0.311	Improvement
Bus Invert (72-bit single-block)	α = 0.296	-4.82%
hihrTS (72-bit single-block)	α = 0.512	+64.63%
Bus Invert (8-bit composed system)	α = 0.249	-19.94%
hihrTS (8-bit composed system)	α = 0.552	+77.50%
XOR PR (72-bit single-block)	α = 0.298	-4.18%

5. Comparison of power consumption on single link

A complete comparison of different study cases to estimate power saving has been carried out.
Data are collected for the encoder-decoder couples able to work at a nominal frequency, synthesized through different DSM technologies, assuming the following model:

$$P = P_{overhead} + N\alpha C_L V_{swing}^2 f_{ck} + R\alpha_R C_L V_{swing}^2 f_{ck}$$

where $P_{overhead}$ is the power consumption of the modules (synthesized with the proper load and correspondent technology at the nominal frequency f_{ck}) N is the number of bits of the formal bus, R denotes the number of flag lines (redundancy). For simplicity, *flag lines' switching activity* α_R *= 50% is assumed and* $P_{overhead}$ *is computed with* α_{INPUT_BUS} *= 50%.*
Power consumption due to redundancy lines never exceeds 10% in the simulations, so these assumptions can be considered reliable.
Proper characterization of the switching activity α_R for the redundancy lines has been performed on the segmented version of Bus Inverter, showing the following results:

Format	Switching activity
MP3	0,452
PDF	0,399
JPG	0,442
TXT	0,115
WMV	0,444
YUV-CIF	0,145
YUV-QCIF	0,162

The characterization has been performed for generic values and wires of different lengths and metal levels, showing major relevance of the capacitive load. Reference power value is chosen as the dynamic power consumption of the bus when no encoder/decoder module is connected

$$P = N\alpha_{ref} C_L V_{swing}^2 f_{ck}$$

Collected data show that only those techniques capable of relevant reductions in switching activity (segmented BI in particular) manage to sustain the hard expense of power arising from the mere presence of the encoder-decoder system, and thus to provide a reduction in energy consumption.

Subsequently, performance may differ dramatically for each trace and for each encoder-decoder couple, depending on how effective the module is on the given data pattern.

Load capacitance plays an important role, as well: heavily charged buses perform better than light ones, and only the final stage of the encoder module is affected. In general, this is the determinant factor in modules' performance and the *break-even point is found in 1.5 pF (approximately 1 mm wire in 65 nm metal 8) for segmented Bus Inverter, which proved the most effective technique* (see below). As far as working frequencies are concerned, it is shown that study cases at lower frequencies tend to provide better performance, though difference can be considered slight.

Data are not collected for University of Catania's variant of Bus Inverter, because this evaluation is inaccurate for the cited technique.

Following data assume 0.5 pF as bus load and 0.1 pF as internal chip load for common data formats.

Tech (nm)	65
Load (pF)	0,5
Supply (V)	1,1
Frequency (MHz)	**200**
Switching activity	**0,492**
Bus size	72
Load scale factor	1
Reference (mW)	4,29
	MP3

Project	Switching activity	Redundancy
BI 72	0,448	1
BI 8	0,361	9
HIHRTS 72	0,488	0
HIHRTS 8	0,486	0
XOR 72	0,493	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,6	3,90	0,06	5,56	29,60%
1,03	3,15	0,54	4,72	10,11%
1,59	4,25	0,00	5,84	36,28%
1,49	4,23	0,00	5,72	33,54%
1,11	4,30	0,00	5,41	26,10%
mW	mW	mW	mW	

Tech (nm)	65
Load (pF)	0,5
Supply (V)	1,1
Frequency (MHz)	**200**
Switching activity	**0,464**
Bus size	72
Load scale factor	1
Reference (mW)	4,04
	PDF

Project	Switching activity	Redundancy
BI 72	0,429	1
BI 8	0,352	9
HIHRTS 72	0,478	0
HIHRTS 8	0,48	0
XOR 72	0,481	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,6	3,74	0,06	5,40	33,53%
1,03	3,07	0,54	4,64	14,81%
1,59	4,16	0,00	5,75	42,35%
1,49	4,18	0,00	5,67	40,31%
1,11	4,19	0,00	5,30	31,12%
mW	mW	mW	mW	

Tech (nm)	65
Load (pF)	0,5
Supply (V)	1,1
Frequency (MHz)	**200**
Switching activity	**0,488**
Bus size	72
Load scale factor	1
Reference (mW)	4,25
	JPG

Project	Switching activity	Redundancy
BI 72	0,444	1
BI 8	0,359	9
HIHRTS 72	0,491	0
HIHRTS 8	0,492	0
XOR 72	0,489	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,6	3,87	0,06	5,53	30,04%
1,03	3,13	0,54	4,70	10,60%
1,59	4,28	0,00	5,87	38,01%
1,49	4,29	0,00	5,78	35,87%
1,11	4,26	0,00	5,37	26,31%
mW	mW	mW	mW	

Tech (nm)	65
Load (pF)	0,5
Supply (V)	1,1
Frequency (MHz)	**200**
Switching activity	**0,327**
Bus size	72
Load scale factor	1
Reference (mW)	2,85
	TXT

Project	Switching activity	Redundancy
BI 72	0,327	1
BI 8	0,31	9
HIHRTS 72	0,478	0
HIHRTS 8	0,478	0
XOR 72	0,403	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,6	2,85	0,06	4,51	58,29%
1,03	2,70	0,54	4,28	50,07%
1,59	4,16	0,00	5,75	101,99%
1,49	4,16	0,00	5,65	98,48%
1,11	3,51	0,00	4,62	62,21%
mW	mW	mW	mW	

Tech (nm)	65
Load (pF)	0,5
Supply (V)	1,1
Frequency (MHz)	**200**
Switching activity	**0,488**
Bus size	72
Load scale factor	1
Reference (mW)	4,25
	WMV

Project	Switching activity	Redundancy
BI 72	0,445	1
BI 8	0,358	9
HIHRTS 72	0,485	0
HIHRTS 8	0,481	0
XOR 72	0,49	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,6	3,88	0,06	5,54	30,25%
1,03	3,12	0,54	4,69	10,40%
1,59	4,23	0,00	5,82	36,78%
1,49	4,19	0,00	5,68	33,61%
1,11	4,27	0,00	5,38	26,52%
mW	mW	mW	mW	

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1	BI 8	0,361	9	2,31	6,29	1,09	9,69	13,02%
Frequency (MHz)	**400**	HIHRTS 72	0,488	0	3,15	8,50	0,00	11,65	35,93%
Switching activity	**0,492**	HIHRTS 8	0,486	0	3	8,47	0,00	11,47	33,78%
Bus size	72	XOR 72	0,493	0	1,8	8,59	0,00	10,39	21,20%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	8,57								
	MP3								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1	BI 8	0,352	9	2,31	6,13	1,09	9,53	17,90%
Frequency (MHz)	**400**	HIHRTS 72	0,478	0	3,15	8,33	0,00	11,48	41,98%
Switching activity	**0,464**	HIHRTS 8	0,48	0	3	8,36	0,00	11,36	40,56%
Bus size	72	XOR 72	0,481	0	1,8	8,38	0,00	10,18	25,93%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	8,08								
	PDF								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1	BI 8	0,359	9	2,31	6,26	1,09	9,65	13,54%
Frequency (MHz)	**400**	HIHRTS 72	0,491	0	3,15	8,56	0,00	11,71	37,66%
Switching activity	**0,488**	HIHRTS 8	0,492	0	3	8,57	0,00	11,57	36,10%
Bus size	72	XOR 72	0,489	0	1,8	8,52	0,00	10,32	21,37%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	8,50								
	JPG								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1	BI 8	0,31	9	2,31	5,40	1,09	8,80	54,46%
Frequency (MHz)	**400**	HIHRTS 72	0,478	0	3,15	8,33	0,00	11,48	101,46%
Switching activity	**0,327**	HIHRTS 8	0,478	0	3	8,33	0,00	11,33	98,83%
Bus size	72	XOR 72	0,403	0	1,8	7,02	0,00	8,82	54,83%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	5,70								
	TXT								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1	BI 8	0,358	9	2,31	6,24	1,09	9,64	13,34%
Frequency (MHz)	**400**	HIHRTS 72	0,485	0	3,15	8,45	0,00	11,60	36,43%
Switching activity	**0,488**	HIHRTS 8	0,481	0	3	8,38	0,00	11,38	33,85%
Bus size	72	XOR 72	0,49	0	1,8	8,54	0,00	10,34	21,58%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	8,50								
	WMV								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1	BI 8	0,361	9	3,09	7,86	1,36	12,31	14,91%
Frequency (MHz)	**500**	HIHRTS 72	0,488	0	3,94	10,63	0,00	14,57	35,96%
Switching activity	**0,492**	HIHRTS 8	0,486	0	3,75	10,59	0,00	14,34	33,78%
Bus size	72	XOR 72	0,493	0	2,25	10,74	0,00	12,99	21,20%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	10,72								
	MP3								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1	BI 8	0,352	9	3,09	7,67	1,36	12,12	19,91%
Frequency (MHz)	**500**	HIHRTS 72	0,478	0	3,94	10,41	0,00	14,35	42,00%
Switching activity	**0,464**	HIHRTS 8	0,48	0	3,75	10,45	0,00	14,20	40,56%
Bus size	72	XOR 72	0,481	0	2,25	10,48	0,00	12,73	25,93%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	10,11								
	PDF								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1	BI 8	0,359	9	3,09	7,82	1,36	12,27	15,45%
Frequency (MHz)	**500**	HIHRTS 72	0,491	0	3,94	10,69	0,00	14,63	37,68%
Switching activity	**0,488**	HIHRTS 8	0,492	0	3,75	10,72	0,00	14,47	36,10%
Bus size	72	XOR 72	0,489	0	2,25	10,65	0,00	12,90	21,37%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	10,63								
	JPG								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1	BI 8	0,31	9	3,09	6,75	1,36	11,20	57,30%
Frequency (MHz)	**500**	HIHRTS 72	0,478	0	3,94	10,41	0,00	14,35	101,50%
Switching activity	**0,327**	HIHRTS 8	0,478	0	3,75	10,41	0,00	14,16	98,83%
Bus size	72	XOR 72	0,403	0	2,25	8,78	0,00	11,03	54,83%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	7,12								
	TXT								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1	BI 8	0,358	9	3,09	7,80	1,36	12,25	15,24%
Frequency (MHz)	**500**	HIHRTS 72	0,485	0	3,94	10,56	0,00	14,50	36,45%
Switching activity	**0,488**	HIHRTS 8	0,481	0	3,75	10,48	0,00	14,23	33,85%
Bus size	72	XOR 72	0,49	0	2,25	10,67	0,00	12,92	21,58%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	10,63								
	WMV								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1								
Frequency (MHz)	**600**	HIHRTS 72	0,488	0	4,72	12,75	0,00	17,47	35,89%
Switching activity	**0,492**	HIHRTS 8	0,486	0	4,49	12,70	0,00	17,19	33,70%
Bus size	72	XOR 72	0,493	0	2,69	12,89	0,00	15,58	21,12%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	12,86								
	MP3								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1								
Frequency (MHz)	**600**	HIHRTS 72	0,478	0	4,72	12,49	0,00	17,21	41,94%
Switching activity	**0,464**	HIHRTS 8	0,48	0	4,49	12,55	0,00	17,04	40,47%
Bus size	72	XOR 72	0,481	0	2,69	12,57	0,00	15,26	25,85%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	12,13								
	PDF								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1								
Frequency (MHz)	**600**	HIHRTS 72	0,491	0	4,72	12,83	0,00	17,55	37,62%
Switching activity	**0,488**	HIHRTS 8	0,492	0	4,49	12,86	0,00	17,35	36,02%
Bus size	72	XOR 72	0,489	0	2,69	12,78	0,00	15,47	21,30%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	12,75								
	JPG								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1								
Frequency (MHz)	**600**	HIHRTS 72	0,478	0	4,72	12,49	0,00	17,21	101,40%
Switching activity	**0,327**	HIHRTS 8	0,478	0	4,49	12,49	0,00	16,98	98,71%
Bus size	72	XOR 72	0,403	0	2,69	10,53	0,00	13,22	54,72%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	8,55								
	TXT								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1								
Frequency (MHz)	**600**	HIHRTS 72	0,485	0	4,72	12,68	0,00	17,40	36,39%
Switching activity	**0,488**	HIHRTS 8	0,481	0	4,49	12,57	0,00	17,06	33,77%
Bus size	72	XOR 72	0,49	0	2,69	12,81	0,00	15,50	21,50%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	12,75								
	WMV								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1								
Frequency (MHz)	**750**	HIHRTS 72	0,488	0	5,94	15,94	0,00	21,88	36,14%
Switching activity	**0,492**	HIHRTS 8	0,486	0	5,65	15,88	0,00	21,53	33,93%
Bus size	72	XOR 72	0,493	0	3,39	16,11	0,00	19,50	21,29%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	16,07								
	MP3								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1								
Frequency (MHz)	**750**	HIHRTS 72	0,478	0	5,94	15,62	0,00	21,56	42,20%
Switching activity	**0,464**	HIHRTS 8	0,48	0	5,65	15,68	0,00	21,33	40,72%
Bus size	72	XOR 72	0,481	0	3,39	15,71	0,00	19,10	26,03%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	15,16								
	PDF								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1								
Frequency (MHz)	**750**	HIHRTS 72	0,491	0	5,94	16,04	0,00	21,98	37,87%
Switching activity	**0,488**	HIHRTS 8	0,492	0	5,65	16,07	0,00	21,72	36,26%
Bus size	72	XOR 72	0,489	0	3,39	15,98	0,00	19,37	21,47%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	15,94								
	JPG								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1								
Frequency (MHz)	**750**	HIHRTS 72	0,478	0	5,94	15,62	0,00	21,56	101,78%
Switching activity	**0,327**	HIHRTS 8	0,478	0	5,65	15,62	0,00	21,27	99,06%
Bus size	72	XOR 72	0,403	0	3,39	13,17	0,00	16,56	54,97%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	10,68								
	TXT								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1								
Frequency (MHz)	**750**	HIHRTS 72	0,485	0	5,94	15,84	0,00	21,78	36,64%
Switching activity	**0,488**	HIHRTS 8	0,481	0	5,65	15,71	0,00	21,36	34,00%
Bus size	72	XOR 72	0,49	0	3,39	16,01	0,00	19,40	21,67%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	15,94								
	WMV								

Tech (nm)	40
Load (pF)	0,5
Supply (V)	1,05
Frequency (MHz)	**200**
Switching activity	**0,492**
Bus size	72
Load scale factor	1
Reference (mW)	3,91
	MP3

Project	Switching activity	Redundancy
BI 72	0,448	1
BI 8	0,361	9
HIHRTS 72	0,488	0
HIHRTS 8	0,486	0
XOR 72	0,493	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,26	3,56	0,06	4,87	24,73%
0,78	2,87	0,50	4,14	6,05%
1,26	3,87	0,00	5,13	31,45%
1,19	3,86	0,00	5,05	29,25%
0,7	3,91	0,00	4,61	18,13%
mW	mW	mW	mW	

Tech (nm)	40
Load (pF)	0,5
Supply (V)	1,05
Frequency (MHz)	**200**
Switching activity	**0,464**
Bus size	72
Load scale factor	1
Reference (mW)	3,68
	PDF

Project	Switching activity	Redundancy
BI 72	0,429	1
BI 8	0,352	9
HIHRTS 72	0,478	0
HIHRTS 8	0,48	0
XOR 72	0,481	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,26	3,41	0,06	4,72	28,16%
0,78	2,79	0,50	4,07	10,51%
1,26	3,79	0,00	5,05	37,23%
1,19	3,81	0,00	5,00	35,76%
0,7	3,82	0,00	4,52	22,67%
mW	mW	mW	mW	

Tech (nm)	40
Load (pF)	0,5
Supply (V)	1,05
Frequency (MHz)	**200**
Switching activity	**0,488**
Bus size	72
Load scale factor	1
Reference (mW)	3,87
	JPG

Project	Switching activity	Redundancy
BI 72	0,444	1
BI 8	0,359	9
HIHRTS 72	0,491	0
HIHRTS 8	0,492	0
XOR 72	0,489	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,26	3,52	0,06	4,84	24,93%
0,78	2,85	0,50	4,13	6,51%
1,26	3,90	0,00	5,16	33,14%
1,19	3,91	0,00	5,10	31,54%
0,7	3,88	0,00	4,58	18,28%
mW	mW	mW	mW	

Tech (nm)	40
Load (pF)	0,5
Supply (V)	1,05
Frequency (MHz)	**200**
Switching activity	**0,327**
Bus size	72
Load scale factor	1
Reference (mW)	2,60
	TXT

Project	Switching activity	Redundancy
BI 72	0,327	1
BI 8	0,31	9
HIHRTS 72	0,478	0
HIHRTS 8	0,478	0
XOR 72	0,403	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,26	2,60	0,06	3,91	50,67%
0,78	2,46	0,50	3,74	43,96%
1,26	3,79	0,00	5,05	94,72%
1,19	3,79	0,00	4,98	92,02%
0,7	3,20	0,00	3,90	50,21%
mW	mW	mW	mW	

Tech (nm)	40
Load (pF)	0,5
Supply (V)	1,05
Frequency (MHz)	**200**
Switching activity	**0,488**
Bus size	72
Load scale factor	1
Reference (mW)	3,87
	WMV

Project	Switching activity	Redundancy
BI 72	0,445	1
BI 8	0,358	9
HIHRTS 72	0,485	0
HIHRTS 8	0,481	0
XOR 72	0,49	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,26	3,53	0,06	4,85	25,14%
0,78	2,84	0,50	4,12	6,30%
1,26	3,85	0,00	5,11	31,91%
1,19	3,82	0,00	5,01	29,29%
0,7	3,89	0,00	4,59	18,48%
mW	mW	mW	mW	

Tech (nm)	40
Load (pF)	0,5
Supply (V)	1,05
Frequency (MHz)	**400**
Switching activity	**0,492**
Bus size	72
Load scale factor	1
Reference (mW)	7,81
	MP3

Project	Switching activity	Redundancy
BI 8	0,361	9
HIHRTS 72	0,488	0
HIHRTS 8	0,486	0
XOR 72	0,493	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,74	5,73	0,99	8,46	8,35%
2,53	7,75	0,00	10,28	31,58%
2,37	7,72	0,00	10,09	29,12%
1,4	7,83	0,00	9,23	18,13%
mW	mW	mW	mW	

Tech (nm)	40
Load (pF)	0,5
Supply (V)	1,05
Frequency (MHz)	**400**
Switching activity	**0,464**
Bus size	72
Load scale factor	1
Reference (mW)	7,37
	PDF

Project	Switching activity	Redundancy
BI 8	0,352	9
HIHRTS 72	0,478	0
HIHRTS 8	0,48	0
XOR 72	0,481	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,74	5,59	0,99	8,32	12,95%
2,53	7,59	0,00	10,12	37,36%
2,37	7,62	0,00	9,99	35,62%
1,4	7,64	0,00	9,04	22,67%
mW	mW	mW	mW	

Tech (nm)	40
Load (pF)	0,5
Supply (V)	1,05
Frequency (MHz)	**400**
Switching activity	**0,488**
Bus size	72
Load scale factor	1
Reference (mW)	7,75
	JPG

Project	Switching activity	Redundancy
BI 8	0,359	9
HIHRTS 72	0,491	0
HIHRTS 8	0,492	0
XOR 72	0,489	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,74	5,70	0,99	8,43	8,83%
2,53	7,80	0,00	10,33	33,27%
2,37	7,81	0,00	10,18	31,41%
1,4	7,76	0,00	9,16	18,28%
mW	mW	mW	mW	

Tech (nm)	40
Load (pF)	0,5
Supply (V)	1,05
Frequency (MHz)	**400**
Switching activity	**0,327**
Bus size	72
Load scale factor	1
Reference (mW)	5,19
	TXT

Project	Switching activity	Redundancy
BI 8	0,31	9
HIHRTS 72	0,478	0
HIHRTS 8	0,478	0
XOR 72	0,403	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,74	4,92	0,99	7,65	47,43%
2,53	7,59	0,00	10,12	94,91%
2,37	7,59	0,00	9,96	91,83%
1,4	6,40	0,00	7,80	50,21%
mW	mW	mW	mW	

Tech (nm)	40
Load (pF)	0,5
Supply (V)	1,05
Frequency (MHz)	**400**
Switching activity	**0,488**
Bus size	72
Load scale factor	1
Reference (mW)	7,75
	WMV

Project	Switching activity	Redundancy
BI 8	0,358	9
HIHRTS 72	0,485	0
HIHRTS 8	0,481	0
XOR 72	0,49	0
		#lines

Overhead	Bus power	Redundancy power	Total power	Improvement
1,74	5,68	0,99	8,42	8,63%
2,53	7,70	0,00	10,23	32,04%
2,37	7,64	0,00	10,01	29,16%
1,4	7,78	0,00	9,18	18,48%
mW	mW	mW	mW	

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,361	9	2,26	7,16	1,24	10,66	9,22%
Frequency (MHz)	**500**	HIHRTS 72	0,488	0	3,15	9,68	0,00	12,83	31,45%
Switching activity	**0,492**	HIHRTS 8	0,486	0	2,97	9,64	0,00	12,61	29,20%
Bus size	72	XOR 72	0,493	0	1,75	9,78	0,00	11,53	18,13%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	9,76								
	MP3								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,352	9	2,26	6,99	1,24	10,49	13,88%
Frequency (MHz)	**500**	HIHRTS 72	0,478	0	3,15	9,49	0,00	12,64	37,23%
Switching activity	**0,464**	HIHRTS 8	0,48	0	2,97	9,53	0,00	12,50	35,70%
Bus size	72	XOR 72	0,481	0	1,75	9,55	0,00	11,30	22,67%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	9,21								
	PDF								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,359	9	2,26	7,12	1,24	10,62	9,71%
Frequency (MHz)	**500**	HIHRTS 72	0,491	0	3,15	9,74	0,00	12,89	33,14%
Switching activity	**0,488**	HIHRTS 8	0,492	0	2,97	9,76	0,00	12,73	31,49%
Bus size	72	XOR 72	0,489	0	1,75	9,70	0,00	11,45	18,28%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	9,68								
	JPG								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,31	9	2,26	6,15	1,24	9,65	48,74%
Frequency (MHz)	**500**	HIHRTS 72	0,478	0	3,15	9,49	0,00	12,64	94,72%
Switching activity	**0,327**	HIHRTS 8	0,478	0	2,97	9,49	0,00	12,46	91,94%
Bus size	72	XOR 72	0,403	0	1,75	8,00	0,00	9,75	50,21%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	6,49								
	TXT								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,358	9	2,26	7,10	1,24	10,60	9,50%
Frequency (MHz)	**500**	HIHRTS 72	0,485	0	3,15	9,62	0,00	12,77	31,91%
Switching activity	**0,488**	HIHRTS 8	0,481	0	2,97	9,55	0,00	12,52	29,23%
Bus size	72	XOR 72	0,49	0	1,75	9,72	0,00	11,47	18,48%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	9,68								
	WMV								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,361	9	2,81	8,60	1,49	12,90	10,06%
Frequency (MHz)	**600**	HIHRTS 72	0,488	0	3,77	11,62	0,00	15,39	31,36%
Switching activity	**0,492**	HIHRTS 8	0,486	0	3,55	11,57	0,00	15,12	29,08%
Bus size	72	XOR 72	0,493	0	2,1	11,74	0,00	13,84	19,13%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	11,72								
	MP3								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,361	9	2,81	8,60	1,49	12,90	16,70%
Frequency (MHz)	**600**	HIHRTS 72	0,478	0	3,77	11,38	0,00	15,15	37,14%
Switching activity	**0,464**	HIHRTS 8	0,48	0	3,55	11,43	0,00	14,98	35,56%
Bus size	72	XOR 72	0,481	0	2,1	11,45	0,00	13,55	22,67%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	11,05								
	PDF								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,361	9	2,81	8,60	1,49	12,90	10,96%
Frequency (MHz)	**600**	HIHRTS 72	0,491	0	3,77	11,69	0,00	15,46	33,06%
Switching activity	**0,488**	HIHRTS 8	0,492	0	3,55	11,72	0,00	15,27	31,37%
Bus size	72	XOR 72	0,489	0	2,1	11,65	0,00	13,75	18,28%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	11,62								
	JPG								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,361	9	2,81	8,60	1,49	12,90	65,60%
Frequency (MHz)	**600**	HIHRTS 72	0,478	0	3,77	11,38	0,00	15,15	94,59%
Switching activity	**0,327**	HIHRTS 8	0,478	0	3,55	11,38	0,00	14,93	91,77%
Bus size	72	XOR 72	0,403	0	2,1	9,60	0,00	11,70	50,21%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	7,79								
	TXT								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,361	9	2,81	8,60	1,49	12,90	10,96%
Frequency (MHz)	**600**	HIHRTS 72	0,485	0	3,77	11,55	0,00	15,32	31,83%
Switching activity	**0,488**	HIHRTS 8	0,481	0	3,55	11,45	0,00	15,00	29,11%
Bus size	72	XOR 72	0,49	0	2,1	11,67	0,00	13,77	18,48%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	11,62								
	WMV								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05								
Frequency (MHz)	**750**	HIHRTS 72	0,488	0	4,75	14,53	0,00	19,28	31,62%
Switching activity	**0,492**	HIHRTS 8	0,486	0	4,47	14,47	0,00	18,94	29,30%
Bus size	72	XOR 72	0,493	0	2,64	14,68	0,00	17,32	18,23%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	14,65								
	MP3								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05								
Frequency (MHz)	**750**	HIHRTS 72	0,478	0	4,75	14,23	0,00	18,98	37,41%
Switching activity	**0,464**	HIHRTS 8	0,48	0	4,47	14,29	0,00	18,76	35,81%
Bus size	72	XOR 72	0,481	0	2,64	14,32	0,00	16,96	22,78%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	13,81								
	PDF								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05								
Frequency (MHz)	**750**	HIHRTS 72	0,491	0	4,75	14,62	0,00	19,37	33,31%
Switching activity	**0,488**	HIHRTS 8	0,492	0	4,47	14,65	0,00	19,12	31,59%
Bus size	72	XOR 72	0,489	0	2,64	14,56	0,00	17,20	18,38%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	14,53								
	JPG								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05								
Frequency (MHz)	**750**	HIHRTS 72	0,478	0	4,75	14,23	0,00	18,98	94,98%
Switching activity	**0,327**	HIHRTS 8	0,478	0	4,47	14,23	0,00	18,70	92,10%
Bus size	72	XOR 72	0,403	0	2,64	12,00	0,00	14,64	50,36%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	9,73								
	TXT								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05								
Frequency (MHz)	**750**	HIHRTS 72	0,485	0	4,75	14,44	0,00	19,19	32,08%
Switching activity	**0,488**	HIHRTS 8	0,481	0	4,47	14,32	0,00	18,79	29,34%
Bus size	72	XOR 72	0,49	0	2,64	14,59	0,00	17,23	18,58%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	14,53								
	WMV								

		Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Tech (nm)	32	BI 72	0,448	1	0,98	2,61	0,04	3,63	26,62%
Load (pF)	0,5	BI 8	0,361	9	0,62	2,11	0,36	3,09	7,68%
Supply (V)	0,9	HIHRTS 72	0,488	0	0,97	2,85	0,00	3,82	32,99%
Frequency (MHz)	**200**	HIHRTS 8	0,486	0	0,92	2,83	0,00	3,75	30,84%
Switching activity	**0,492**	XOR 72	0,493	0	0,55	2,88	0,00	3,43	19,37%
Bus size	72			#lines	mW	mW	mW	mW	
Load scale factor	1								
Reference (mW)	2,87								
	MP3								

		Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Tech (nm)	32	BI 72	0,429	1	0,98	2,50	0,04	3,52	30,17%
Load (pF)	0,5	BI 8	0,352	9	0,62	2,05	0,36	3,04	12,24%
Supply (V)	0,9	HIHRTS 72	0,478	0	0,97	2,79	0,00	3,76	38,86%
Frequency (MHz)	**200**	HIHRTS 8	0,48	0	0,92	2,80	0,00	3,72	37,45%
Switching activity	**0,464**	XOR 72	0,481	0	0,55	2,81	0,00	3,36	23,99%
Bus size	72			#lines	mW	mW	mW	mW	
Load scale factor	1								
Reference (mW)	2,71								
	PDF								

		Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Tech (nm)	32	BI 72	0,444	1	0,98	2,59	0,04	3,61	26,84%
Load (pF)	0,5	BI 8	0,359	9	0,62	2,09	0,36	3,08	8,16%
Supply (V)	0,9	HIHRTS 72	0,491	0	0,97	2,86	0,00	3,83	34,70%
Frequency (MHz)	**200**	HIHRTS 8	0,492	0	0,92	2,87	0,00	3,79	33,15%
Switching activity	**0,488**	XOR 72	0,489	0	0,55	2,85	0,00	3,40	19,53%
Bus size	72			#lines	mW	mW	mW	mW	
Load scale factor	1								
Reference (mW)	2,85								
	JPG								

		Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Tech (nm)	32	BI 72	0,327	1	0,98	1,91	0,04	2,93	53,51%
Load (pF)	0,5	BI 8	0,31	9	0,62	1,81	0,36	2,79	46,43%
Supply (V)	0,9	HIHRTS 72	0,478	0	0,97	2,79	0,00	3,76	97,04%
Frequency (MHz)	**200**	HIHRTS 8	0,478	0	0,92	2,79	0,00	3,71	94,42%
Switching activity	**0,327**	XOR 72	0,403	0	0,55	2,35	0,00	2,90	52,08%
Bus size	72			#lines	mW	mW	mW	mW	
Load scale factor	1								
Reference (mW)	1,91								
	TXT								

		Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Tech (nm)	32	BI 72	0,445	1	0,98	2,60	0,04	3,62	27,05%
Load (pF)	0,5	BI 8	0,358	9	0,62	2,09	0,36	3,07	7,95%
Supply (V)	0,9	HIHRTS 72	0,485	0	0,97	2,83	0,00	3,80	33,47%
Frequency (MHz)	**200**	HIHRTS 8	0,481	0	0,92	2,81	0,00	3,73	30,89%
Switching activity	**0,488**	XOR 72	0,49	0	0,55	2,86	0,00	3,41	19,74%
Bus size	72			#lines	mW	mW	mW	mW	
Load scale factor	1								
Reference (mW)	2,85								
	WMV								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,361	9	1,26	4,21	0,73	6,20	6,03%
Frequency (MHz)	**400**	HIHRTS 72	0,488	0	1,94	5,69	0,00	7,63	32,99%
Switching activity	**0,492**	HIHRTS 8	0,486	0	1,85	5,67	0,00	7,52	31,02%
Bus size	72	XOR 72	0,493	0	1,12	5,75	0,00	6,87	19,72%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	5,74								
	MP3								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,352	9	1,26	4,11	0,73	6,09	12,61%
Frequency (MHz)	**400**	HIHRTS 72	0,478	0	1,94	5,58	0,00	7,52	38,86%
Switching activity	**0,464**	HIHRTS 8	0,48	0	1,85	5,60	0,00	7,45	37,63%
Bus size	72	XOR 72	0,481	0	1,12	5,61	0,00	6,73	24,36%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	5,41								
	PDF								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,359	9	1,26	4,19	0,73	6,18	8,51%
Frequency (MHz)	**400**	HIHRTS 72	0,491	0	1,94	5,73	0,00	7,67	34,70%
Switching activity	**0,488**	HIHRTS 8	0,492	0	1,85	5,74	0,00	7,59	33,32%
Bus size	72	XOR 72	0,489	0	1,12	5,70	0,00	6,82	19,88%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	5,69								
	JPG								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,31	9	1,26	3,62	0,73	5,60	46,95%
Frequency (MHz)	**400**	HIHRTS 72	0,478	0	1,94	5,58	0,00	7,52	97,04%
Switching activity	**0,327**	HIHRTS 8	0,478	0	1,85	5,58	0,00	7,43	94,68%
Bus size	72	XOR 72	0,403	0	1,12	4,70	0,00	5,82	52,61%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	3,81								
	TXT								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,358	9	1,26	4,18	0,73	6,16	8,30%
Frequency (MHz)	**400**	HIHRTS 72	0,485	0	1,94	5,66	0,00	7,60	33,47%
Switching activity	**0,488**	HIHRTS 8	0,481	0	1,85	5,61	0,00	7,46	31,07%
Bus size	72	XOR 72	0,49	0	1,12	5,72	0,00	6,84	20,09%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	5,69								
	WMV								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,361	9	1,57	5,26	0,91	7,74	7,96%
Frequency (MHz)	**500**	HIHRTS 72	0,488	0	2,45	7,12	0,00	9,57	33,34%
Switching activity	**0,492**	HIHRTS 8	0,486	0	2,33	7,09	0,00	9,42	31,26%
Bus size	72	XOR 72	0,493	0	1,37	7,19	0,00	8,56	19,30%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	7,17								
	MP3								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,352	9	1,57	5,13	0,91	7,61	12,54%
Frequency (MHz)	**500**	HIHRTS 72	0,478	0	2,45	6,97	0,00	9,42	39,23%
Switching activity	**0,464**	HIHRTS 8	0,48	0	2,33	7,00	0,00	9,33	37,89%
Bus size	72	XOR 72	0,481	0	1,37	7,01	0,00	8,38	23,91%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	6,77								
	PDF								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,359	9	1,57	5,23	0,91	7,72	8,44%
Frequency (MHz)	**500**	HIHRTS 72	0,491	0	2,45	7,16	0,00	9,61	35,05%
Switching activity	**0,488**	HIHRTS 8	0,492	0	2,33	7,17	0,00	9,50	33,57%
Bus size	72	XOR 72	0,489	0	1,37	7,13	0,00	8,50	19,46%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	7,12								
	JPG								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,31	9	1,57	4,52	0,91	7,00	46,84%
Frequency (MHz)	**500**	HIHRTS 72	0,478	0	2,45	6,97	0,00	9,42	97,57%
Switching activity	**0,327**	HIHRTS 8	0,478	0	2,33	6,97	0,00	9,30	95,05%
Bus size	72	XOR 72	0,403	0	1,37	5,88	0,00	7,25	51,98%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	4,77								
	TXT								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,358	9	1,57	5,22	0,91	7,70	8,23%
Frequency (MHz)	**500**	HIHRTS 72	0,485	0	2,45	7,07	0,00	9,52	33,82%
Switching activity	**0,488**	HIHRTS 8	0,481	0	2,33	7,01	0,00	9,34	31,31%
Bus size	72	XOR 72	0,49	0	1,37	7,14	0,00	8,51	19,66%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	7,12								
	WMV								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,361	9	2	6,32	1,09	9,41	9,31%
Frequency (MHz)	**600**	HIHRTS 72	0,488	0	2,93	8,54	0,00	11,47	33,22%
Switching activity	**0,492**	HIHRTS 8	0,486	0	2,79	8,50	0,00	11,29	31,19%
Bus size	72	XOR 72	0,493	0	1,64	8,63	0,00	10,27	19,26%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	8,61								
	MP3								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,352	9	2	6,16	1,09	9,25	13,97%
Frequency (MHz)	**600**	HIHRTS 72	0,478	0	2,93	8,36	0,00	11,29	39,11%
Switching activity	**0,464**	HIHRTS 8	0,48	0	2,79	8,40	0,00	11,19	37,82%
Bus size	72	XOR 72	0,481	0	1,64	8,42	0,00	10,06	23,87%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	8,12								
	PDF								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,359	9	2	6,28	1,09	9,37	9,80%
Frequency (MHz)	**600**	HIHRTS 72	0,491	0	2,93	8,59	0,00	11,52	34,93%
Switching activity	**0,488**	HIHRTS 8	0,492	0	2,79	8,61	0,00	11,40	33,50%
Bus size	72	XOR 72	0,489	0	1,64	8,56	0,00	10,20	19,41%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	8,54								
	JPG								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,31	9	2	5,42	1,09	8,52	48,87%
Frequency (MHz)	**600**	HIHRTS 72	0,478	0	2,93	8,36	0,00	11,29	97,39%
Switching activity	**0,327**	HIHRTS 8	0,478	0	2,79	8,36	0,00	11,15	94,94%
Bus size	72	XOR 72	0,403	0	1,64	7,05	0,00	8,69	51,91%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	5,72								
	TXT								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,358	9	2	6,26	1,09	9,36	9,59%
Frequency (MHz)	**600**	HIHRTS 72	0,485	0	2,93	8,49	0,00	11,42	33,70%
Switching activity	**0,488**	HIHRTS 8	0,481	0	2,79	8,42	0,00	11,21	31,24%
Bus size	72	XOR 72	0,49	0	1,64	8,57	0,00	10,21	19,62%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	8,54								
	WMV								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9								
Frequency (MHz)	**750**	HIHRTS 72	0,488	0	3,67	10,67	0,00	14,34	33,29%
Switching activity	**0,492**	HIHRTS 8	0,486	0	3,48	10,63	0,00	14,11	31,12%
Bus size	72	XOR 72	0,493	0	2,06	10,78	0,00	12,84	19,35%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	10,76								
	MP3								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9								
Frequency (MHz)	**750**	HIHRTS 72	0,478	0	3,67	10,45	0,00	14,12	39,18%
Switching activity	**0,464**	HIHRTS 8	0,48	0	3,48	10,50	0,00	13,98	37,74%
Bus size	72	XOR 72	0,481	0	2,06	10,52	0,00	12,58	23,96%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	10,15								
	PDF								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9								
Frequency (MHz)	**750**	HIHRTS 72	0,491	0	3,67	10,74	0,00	14,41	35,00%
Switching activity	**0,488**	HIHRTS 8	0,492	0	3,48	10,76	0,00	14,24	33,43%
Bus size	72	XOR 72	0,489	0	2,06	10,69	0,00	12,75	19,51%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	10,67								
	JPG								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9								
Frequency (MHz)	**750**	HIHRTS 72	0,478	0	3,67	10,45	0,00	14,12	97,50%
Switching activity	**0,327**	HIHRTS 8	0,478	0	3,48	10,45	0,00	13,93	94,84%
Bus size	72	XOR 72	0,403	0	2,06	8,81	0,00	10,87	52,05%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	7,15								
	TXT								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9								
Frequency (MHz)	**750**	HIHRTS 72	0,485	0	3,67	10,61	0,00	14,28	33,77%
Switching activity	**0,488**	HIHRTS 8	0,481	0	3,48	10,52	0,00	14,00	31,17%
Bus size	72	XOR 72	0,49	0	2,06	10,72	0,00	12,78	19,71%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	10,67								
	WMV								

Following data assume 0.5 pF as bus load and 0.1 pF as internal chip load for use in video encoders.

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5	BI 72	0,281	1	1,6	2,45	0,06	4,11	62,06%
Supply (V)	1,1	BI 8	0,233	9	1,03	2,03	0,54	3,60	42,17%
Frequency (MHz)	**200**	HIHRTS 72	0,51	0	1,59	4,44	0,00	6,03	137,97%
Switching activity	**0,291**	HIHRTS 8	0,552	0	1,49	4,81	0,00	6,30	148,46%
Bus size	72	XOR 72	0,281	0	1,11	2,45	0,00	3,56	40,35%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	2,54								
	YUV-CIF								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5	BI 72	0,298	1	1,6	2,58	0,06	4,24	56,46%
Supply (V)	1,1	BI 8	0,249	9	1,03	2,17	0,54	3,74	38,18%
Frequency (MHz)	**200**	HIHRTS 72	0,512	0	1,59	4,46	0,00	6,05	123,31%
Switching activity	**0,311**	HIHRTS 8	0,552	0	1,49	4,81	0,00	6,30	132,49%
Bus size	72	XOR 72	0,298	0	1,11	2,60	0,00	3,71	36,79%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	2,71								
	YUV-QCIF								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1	BI 8	0,233	9	2,31	4,06	1,09	7,46	47,11%
Frequency (MHz)	**400**	HIHRTS 72	0,51	0	3,15	8,89	0,00	12,04	137,38%
Switching activity	**0,291**	HIHRTS 8	0,552	0	3	9,62	0,00	12,62	148,86%
Bus size	72	XOR 72	0,281	0	1,8	4,90	0,00	6,70	32,06%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	5,07								
	YUV-CIF								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1	BI 8	0,249	9	2,31	4,34	1,09	7,74	42,79%
Frequency (MHz)	**400**	HIHRTS 72	0,512	0	3,15	8,92	0,00	12,07	122,76%
Switching activity	**0,311**	HIHRTS 8	0,552	0	3	9,62	0,00	12,62	132,85%
Bus size	72	XOR 72	0,298	0	1,8	5,19	0,00	6,99	29,04%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	5,42								
	YUV-QCIF								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1	BI 8	0,233	9	3,09	5,07	1,36	9,53	50,30%
Frequency (MHz)	**500**	HIHRTS 72	0,51	0	3,94	11,11	0,00	15,05	137,42%
Switching activity	**0,291**	HIHRTS 8	0,552	0	3,75	12,02	0,00	15,77	148,86%
Bus size	72	XOR 72	0,281	0	2,25	6,12	0,00	8,37	32,06%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	6,34								
	YUV-CIF								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1	BI 8	0,249	9	3,09	5,42	1,36	9,87	45,78%
Frequency (MHz)	**500**	HIHRTS 72	0,512	0	3,94	11,15	0,00	15,09	122,80%
Switching activity	**0,311**	HIHRTS 8	0,552	0	3,75	12,02	0,00	15,77	132,85%
Bus size	72	XOR 72	0,298	0	2,25	6,49	0,00	8,74	29,04%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	6,77								
	YUV-QCIF								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1								
Frequency (MHz)	**600**	HIHRTS 72	0,51	0	4,72	13,33	0,00	18,05	137,32%
Switching activity	**0,291**	HIHRTS 8	0,552	0	4,49	14,43	0,00	18,92	148,73%
Bus size	72	XOR 72	0,281	0	2,69	7,34	0,00	10,03	31,93%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	7,61								
	YUV-CIF								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1								
Frequency (MHz)	**600**	HIHRTS 72	0,512	0	4,72	13,38	0,00	18,10	122,70%
Switching activity	**0,311**	HIHRTS 8	0,552	0	4,49	14,43	0,00	18,92	132,73%
Bus size	72	XOR 72	0,298	0	2,69	7,79	0,00	10,48	28,91%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	8,13								
	YUV-QCIF								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1								
Frequency (MHz)	**750**	HIHRTS 72	0,51	0	5,94	16,66	0,00	22,60	137,74%
Switching activity	**0,291**	HIHRTS 8	0,552	0	5,65	18,03	0,00	23,68	149,12%
Bus size	72	XOR 72	0,281	0	3,39	9,18	0,00	12,57	32,22%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	9,51								
	YUV-CIF								

Tech (nm)	65	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,1								
Frequency (MHz)	**750**	HIHRTS 72	0,512	0	4,72	16,73	0,00	21,45	111,09%
Switching activity	**0,311**	HIHRTS 8	0,552	0	4,49	18,03	0,00	22,52	121,68%
Bus size	72	XOR 72	0,298	0	2,69	9,74	0,00	12,43	22,30%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	10,16								
	YUV-QCIF								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5	BI 72	0,281	1	1,26	2,23	0,06	3,55	53,50%
Supply (V)	1,05	BI 8	0,233	9	0,78	1,85	0,50	3,13	35,31%
Frequency (MHz)	**200**	HIHRTS 72	0,51	0	1,26	4,05	0,00	5,31	129,80%
Switching activity	**0,291**	HIHRTS 8	0,552	0	1,19	4,38	0,00	5,57	141,21%
Bus size	72	XOR 72	0,281	0	0,7	2,23	0,00	2,93	26,87%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	2,31								
	YUV-CIF								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5	BI 72	0,296	1	1,26	2,35	0,06	3,66	48,45%
Supply (V)	1,05	BI 8	0,249	9	0,78	1,98	0,50	3,25	31,76%
Frequency (MHz)	**200**	HIHRTS 72	0,512	0	1,26	4,06	0,00	5,32	115,67%
Switching activity	**0,311**	HIHRTS 8	0,552	0	1,19	4,38	0,00	5,57	125,70%
Bus size	72	XOR 72	0,298	0	0,7	2,37	0,00	3,07	24,17%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	2,47								
	YUV-QCIF								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,233	9	1,74	3,70	0,99	6,43	39,21%
Frequency (MHz)	**400**	HIHRTS 72	0,51	0	2,53	8,10	0,00	10,63	130,02%
Switching activity	**0,291**	HIHRTS 8	0,552	0	2,37	8,76	0,00	11,13	140,99%
Bus size	72	XOR 72	0,281	0	1,4	4,46	0,00	5,86	26,87%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	4,62								
	YUV-CIF								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,249	9	1,74	3,95	0,99	6,69	35,40%
Frequency (MHz)	**400**	HIHRTS 72	0,512	0	2,53	8,13	0,00	10,66	115,87%
Switching activity	**0,311**	HIHRTS 8	0,552	0	2,37	8,76	0,00	11,13	125,49%
Bus size	72	XOR 72	0,298	0	1,4	4,73	0,00	6,13	24,17%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	4,94								
	YUV-QCIF								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,233	9	2,26	4,62	1,24	8,12	40,68%
Frequency (MHz)	**500**	HIHRTS 72	0,51	0	3,15	10,12	0,00	13,27	129,80%
Switching activity	**0,291**	HIHRTS 8	0,552	0	2,97	10,95	0,00	13,92	141,12%
Bus size	72	XOR 72	0,281	0	1,75	5,58	0,00	7,33	26,87%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	5,77								
	YUV-CIF								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,249	9	2,26	4,94	1,24	8,44	36,78%
Frequency (MHz)	**500**	HIHRTS 72	0,512	0	3,15	10,16	0,00	13,31	115,67%
Switching activity	**0,311**	HIHRTS 8	0,552	0	2,97	10,95	0,00	13,92	126,61%
Bus size	72	XOR 72	0,298	0	1,75	5,91	0,00	7,66	24,17%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	6,17								
	YUV-QCIF								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,249	9	2,81	5,93	1,49	10,23	47,59%
Frequency (MHz)	**600**	HIHRTS 72	0,51	0	3,77	12,15	0,00	15,92	129,66%
Switching activity	**0,291**	HIHRTS 8	0,552	0	3,55	13,15	0,00	16,70	140,92%
Bus size	72	XOR 72	0,281	0	2,1	6,69	0,00	8,79	26,87%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	6,93								
	YUV-CIF								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05	BI 8	0,249	9	2,81	5,93	1,49	10,23	38,10%
Frequency (MHz)	**600**	HIHRTS 72	0,512	0	3,77	12,19	0,00	15,96	115,53%
Switching activity	**0,311**	HIHRTS 8	0,552	0	3,55	13,15	0,00	16,70	125,43%
Bus size	72	XOR 72	0,298	0	2,1	7,10	0,00	9,20	24,17%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	7,41								
	YUV-QCIF								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05								
Frequency (MHz)	**750**	HIHRTS 72	0,51	0	4,75	15,18	0,00	19,93	130,09%
Switching activity	**0,291**	HIHRTS 8	0,552	0	4,47	16,43	0,00	20,90	141,29%
Bus size	72	XOR 72	0,281	0	2,64	8,36	0,00	11,00	27,04%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	8,66								
	YUV-CIF								

Tech (nm)	40	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	1,05								
Frequency (MHz)	**750**	HIHRTS 72	0,512	0	4,75	15,24	0,00	19,99	115,94%
Switching activity	**0,311**	HIHRTS 8	0,552	0	4,47	16,43	0,00	20,90	125,78%
Bus size	72	XOR 72	0,298	0	2,64	8,87	0,00	11,51	24,34%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	9,26								
	YUV-QCIF								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5	BI 72	0,281	1	0,98	1,64	0,04	2,66	56,70%
Supply (V)	0,9	BI 8	0,233	9	0,62	1,36	0,36	2,34	38,08%
Frequency (MHz)	**200**	HIHRTS 72	0,51	0	0,97	2,97	0,00	3,94	132,41%
Switching activity	**0,291**	HIHRTS 8	0,552	0	0,92	3,22	0,00	4,14	143,90%
Bus size	72	XOR 72	0,281	0	0,55	1,64	0,00	2,19	28,97%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	1,70								
	YUV-CIF								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5	BI 72	0,296	1	0,98	1,73	0,04	2,75	51,44%
Supply (V)	0,9	BI 8	0,249	9	0,62	1,45	0,36	2,44	34,34%
Frequency (MHz)	**200**	HIHRTS 72	0,512	0	0,97	2,99	0,00	3,96	118,11%
Switching activity	**0,311**	HIHRTS 8	0,552	0	0,92	3,22	0,00	4,14	128,22%
Bus size	72	XOR 72	0,298	0	0,55	1,74	0,00	2,29	26,14%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	1,81								
	YUV-QCIF								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,233	9	1,26	2,72	0,73	4,71	38,67%
Frequency (MHz)	**400**	HIHRTS 72	0,51	0	1,94	5,95	0,00	7,89	132,41%
Switching activity	**0,291**	HIHRTS 8	0,552	0	1,85	6,44	0,00	8,29	144,20%
Bus size	72	XOR 72	0,281	0	1,12	3,28	0,00	4,40	29,56%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	3,39								
	YUV-CIF								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,249	9	1,26	2,90	0,73	4,89	34,90%
Frequency (MHz)	**400**	HIHRTS 72	0,512	0	1,94	5,97	0,00	7,91	118,11%
Switching activity	**0,311**	HIHRTS 8	0,552	0	1,85	6,44	0,00	8,29	128,49%
Bus size	72	XOR 72	0,298	0	1,12	3,48	0,00	4,60	26,70%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	3,63								
	YUV-QCIF								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,233	9	1,57	3,40	0,91	5,88	38,55%
Frequency (MHz)	**500**	HIHRTS 72	0,51	0	2,45	7,44	0,00	9,89	133,00%
Switching activity	**0,291**	HIHRTS 8	0,552	0	2,33	8,05	0,00	10,38	144,61%
Bus size	72	XOR 72	0,281	0	1,37	4,10	0,00	5,47	28,95%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	4,24								
	YUV-CIF								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,249	9	1,57	3,63	0,91	6,11	34,79%
Frequency (MHz)	**500**	HIHRTS 72	0,512	0	2,45	7,46	0,00	9,91	118,66%
Switching activity	**0,311**	HIHRTS 8	0,552	0	2,33	8,05	0,00	10,38	128,88%
Bus size	72	XOR 72	0,298	0	1,37	4,34	0,00	5,71	26,03%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	4,53								
	YUV-QCIF								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,249	9	2	4,36	1,09	7,45	46,33%
Frequency (MHz)	**600**	HIHRTS 72	0,51	0	2,93	8,92	0,00	11,85	132,81%
Switching activity	**0,291**	HIHRTS 8	0,552	0	2,79	9,66	0,00	12,45	144,49%
Bus size	72	XOR 72	0,281	0	1,64	4,92	0,00	6,56	28,78%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	5,09								
	YUV-CIF								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9	BI 8	0,249	9	2	4,36	1,09	7,45	36,92%
Frequency (MHz)	**600**	HIHRTS 72	0,512	0	2,93	8,96	0,00	11,89	118,48%
Switching activity	**0,311**	HIHRTS 8	0,552	0	2,79	9,66	0,00	12,45	126,77%
Bus size	72	XOR 72	0,298	0	1,64	5,21	0,00	6,85	25,96%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	5,44								
	YUV-QCIF								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9								
Frequency (MHz)	**750**	HIHRTS 72	0,51	0	3,67	11,15	0,00	14,82	132,92%
Switching activity	**0,291**	HIHRTS 8	0,552	0	3,48	12,07	0,00	15,55	144,37%
Bus size	72	XOR 72	0,281	0	2,06	6,15	0,00	8,21	28,93%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	6,36								
	YUV-CIF								

Tech (nm)	32	Project	Switching activity	Redundancy	Overhead	Bus power	Redundancy power	Total power	Improvement
Load (pF)	0,5								
Supply (V)	0,9								
Frequency (MHz)	**750**	HIHRTS 72	0,512	0	3,67	11,20	0,00	14,87	118,59%
Switching activity	**0,311**	HIHRTS 8	0,552	0	3,48	12,07	0,00	15,55	126,66%
Bus size	72	XOR 72	0,298	0	2,06	6,52	0,00	8,58	26,11%
Load scale factor	1			#lines	mW	mW	mW	mW	
Reference (mW)	6,80								
	YUV-QCIF								

6. Bus Inverter breakeven on single link

Following data show results of simulations on segmented Bus Inverter for typical single-link wire values. As shown above, this general-purpose module outperformed the others in terms of effective power-saving on the vast majority of data formats, though not on raw switching activity reduction and speed.

This testbench assumes 1.0 – 1.5 fF/um (1.0 – 1.5 pF/mm), close to 65-nm upper layers (metal 8). Improvement in power consumption is provided only for long wires; *break-even (in terms of load capacitance) is found around 1.5 pF.*

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	1									
Supply (V)	1,1	MP3	0,492	0,361	6,29	1,48	1,09	8,86	8,57	3,34%
Bus size	72	PDF	0,464	0,352	6,13	1,48	1,09	8,70	8,08	7,64%
Redundancy lines	9	JPG	0,488	0,359	6,26	1,48	1,09	8,82	8,50	3,78%
Frequency (MHz)	**200**	TXT	0,327	0,31	5,40	1,48	1,09	7,97	5,70	39,89%
		WMV	0,488	0,358	6,24	1,48	1,09	8,81	8,50	3,57%
		YUV-CIF	0,291	0,233	4,06	1,48	1,09	6,63	5,07	30,74%
		YUV-QCIF	0,311	0,249	4,34	1,48	1,09	6,91	5,42	27,47%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	1									
Supply (V)	1,1	MP3	0,492	0,361	12,58	3,10	2,18	17,86	17,15	4,16%
Bus size	72	PDF	0,464	0,352	12,27	3,10	2,18	17,54	16,17	8,50%
Redundancy lines	9	JPG	0,488	0,359	12,51	3,10	2,18	17,79	17,01	4,60%
Frequency (MHz)	**400**	TXT	0,327	0,31	10,80	3,10	2,18	16,08	11,40	41,12%
		WMV	0,488	0,358	12,48	3,10	2,18	17,75	17,01	4,40%
		YUV-CIF	0,291	0,233	8,12	3,10	2,18	13,40	10,14	32,12%
		YUV-QCIF	0,311	0,249	8,68	3,10	2,18	13,96	10,84	28,76%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	1									
Supply (V)	1,1	MP3	0,492	0,361	15,73	4,04	2,72	22,49	21,43	4,93%
Bus size	72	PDF	0,464	0,352	15,33	4,04	2,72	22,10	20,21	9,32%
Redundancy lines	9	JPG	0,488	0,359	15,64	4,04	2,72	22,40	21,26	5,38%
Frequency (MHz)	**500**	TXT	0,327	0,31	13,50	4,04	2,72	20,27	14,24	42,28%
		WMV	0,488	0,358	15,59	4,04	2,72	22,36	21,26	5,17%
		YUV-CIF	0,291	0,233	10,15	4,04	2,72	16,91	12,68	33,42%
		YUV-QCIF	0,311	0,249	10,85	4,04	2,72	17,61	13,55	29,98%
					mW	mW	mW	mW	mW	

Data for 1 mm of 1.0 fF/um wire

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	1,5									
Supply (V)	1,1	MP3	0,492	0,361	9,44	1,93	1,63	13,00	12,86	1,09%
Bus size	72	PDF	0,464	0,352	9,20	1,93	1,63	12,76	12,13	5,25%
Redundancy lines	9	JPG	0,488	0,359	9,38	1,93	1,63	12,95	12,75	1,51%
Frequency (MHz)	**200**	TXT	0,327	0,31	8,10	1,93	1,63	11,67	8,55	36,50%
		WMV	0,488	0,358	9,36	1,93	1,63	12,92	12,75	1,30%
		YUV-CIF	0,291	0,233	6,09	1,93	1,63	9,65	7,61	26,92%
		YUV-QCIF	0,311	0,249	6,51	1,93	1,63	10,07	8,13	23,90%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	1,5									
Supply (V)	1,1	MP3	0,492	0,361	18,87	4,13	3,27	26,27	25,72	2,14%
Bus size	72	PDF	0,464	0,352	18,40	4,13	3,27	25,80	24,25	6,36%
Redundancy lines	9	JPG	0,488	0,359	18,77	4,13	3,27	26,16	25,51	2,56%
Frequency (MHz)	**400**	TXT	0,327	0,31	16,20	4,13	3,27	23,60	17,09	38,08%
		WMV	0,488	0,358	18,71	4,13	3,27	26,11	25,51	2,36%
		YUV-CIF	0,291	0,233	12,18	4,13	3,27	19,58	15,21	28,70%
		YUV-QCIF	0,311	0,249	13,02	4,13	3,27	20,41	16,26	25,57%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	1,5									
Supply (V)	1,1	MP3	0,492	0,361	23,59	5,16	4,08	32,83	32,15	2,13%
Bus size	72	PDF	0,464	0,352	23,00	5,16	4,08	32,24	30,32	6,35%
Redundancy lines	9	JPG	0,488	0,359	23,46	5,16	4,08	32,70	31,89	2,56%
Frequency (MHz)	**500**	TXT	0,327	0,31	20,26	5,16	4,08	29,50	21,37	38,06%
		WMV	0,488	0,358	23,39	5,16	4,08	32,64	31,89	2,35%
		YUV-CIF	0,291	0,233	15,22	5,16	4,08	24,47	19,01	28,68%
		YUV-QCIF	0,311	0,249	16,27	5,16	4,08	25,51	20,32	25,55%
					mW	mW	mW	mW	mW	

Data for 1.5 mm of 1.0 fF/um wire

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	2									
Supply (V)	1,1	MP3	0,492	0,361	12,58	2,38	2,18	17,14	17,15	-0,04%
Bus size	72	PDF	0,464	0,352	12,27	2,38	2,18	16,82	16,17	4,05%
Redundancy lines	9	JPG	0,488	0,359	12,51	2,38	2,18	17,07	17,01	0,37%
Frequency (MHz)	**200**	TXT	0,327	0,31	10,80	2,38	2,18	15,36	11,40	34,80%
		WMV	0,488	0,358	12,48	2,38	2,18	17,03	17,01	0,16%
		YUV-CIF	0,291	0,233	8,12	2,38	2,18	12,68	10,14	25,02%
		YUV-QCIF	0,311	0,249	8,68	2,38	2,18	13,24	10,84	22,12%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	2									
Supply (V)	1,1	MP3	0,492	0,361	25,16	4,90	4,36	34,42	34,29	0,37%
Bus size	72	PDF	0,464	0,352	24,53	4,90	4,36	33,79	32,34	4,48%
Redundancy lines	9	JPG	0,488	0,359	25,02	4,90	4,36	34,28	34,01	0,78%
Frequency (MHz)	**400**	TXT	0,327	0,31	21,61	4,90	4,36	30,86	22,79	35,41%
		WMV	0,488	0,358	24,95	4,90	4,36	34,21	34,01	0,57%
		YUV-CIF	0,291	0,233	16,24	4,90	4,36	25,50	20,28	25,71%
		YUV-QCIF	0,311	0,249	17,35	4,90	4,36	26,61	21,68	22,77%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	2									
Supply (V)	1,1	MP3	0,492	0,361	31,45	6,54	5,45	43,44	42,86	1,34%
Bus size	72	PDF	0,464	0,352	30,67	6,54	5,45	42,65	40,42	5,51%
Redundancy lines	9	JPG	0,488	0,359	31,28	6,54	5,45	43,26	42,51	1,76%
Frequency (MHz)	**500**	TXT	0,327	0,31	27,01	6,54	5,45	38,99	28,49	36,87%
		WMV	0,488	0,358	31,19	6,54	5,45	43,17	42,51	1,55%
		YUV-CIF	0,291	0,233	20,30	6,54	5,45	32,28	25,35	27,34%
		YUV-QCIF	0,311	0,249	21,69	6,54	5,45	33,68	27,09	24,30%
					mW	mW	mW	mW	mW	

Data for 2 mm of 1.0 fF/um wire

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	2,5									
Supply (V)	1,1	MP3	0,492	0,361	15,73	2,83	2,72	21,28	21,43	-0,72%
Bus size	72	PDF	0,464	0,352	15,33	2,83	2,72	20,89	20,21	3,33%
Redundancy lines	9	JPG	0,488	0,359	15,64	2,83	2,72	21,19	21,26	-0,31%
Frequency (MHz)	**200**	TXT	0,327	0,31	13,50	2,83	2,72	19,06	14,24	33,78%
		WMV	0,488	0,358	15,59	2,83	2,72	21,15	21,26	-0,52%
		YUV-CIF	0,291	0,233	10,15	2,83	2,72	15,70	12,68	23,87%
		YUV-QCIF	0,311	0,249	10,85	2,83	2,72	16,40	13,55	21,05%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	2,5									
Supply (V)	1,1	MP3	0,492	0,361	31,45	5,78	5,45	42,68	42,86	-0,44%
Bus size	72	PDF	0,464	0,352	30,67	5,78	5,45	41,89	40,42	3,63%
Redundancy lines	9	JPG	0,488	0,359	31,28	5,78	5,45	42,50	42,51	-0,03%
Frequency (MHz)	**400**	TXT	0,327	0,31	27,01	5,78	5,45	38,23	28,49	34,20%
		WMV	0,488	0,358	31,19	5,78	5,45	42,41	42,51	-0,24%
		YUV-CIF	0,291	0,233	20,30	5,78	5,45	31,52	25,35	24,35%
		YUV-QCIF	0,311	0,249	21,69	5,78	5,45	32,92	27,09	21,49%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	2,5									
Supply (V)	1,1	MP3	0,492	0,361	39,31	7,50	6,81	53,62	53,58	0,08%
Bus size	72	PDF	0,464	0,352	38,33	7,50	6,81	52,64	50,53	4,17%
Redundancy lines	9	JPG	0,488	0,359	39,10	7,50	6,81	53,40	53,14	0,49%
Frequency (MHz)	**500**	TXT	0,327	0,31	33,76	7,50	6,81	48,07	35,61	34,98%
		WMV	0,488	0,358	38,99	7,50	6,81	53,29	53,14	0,28%
		YUV-CIF	0,291	0,233	25,37	7,50	6,81	39,68	31,69	25,21%
		YUV-QCIF	0,311	0,249	27,12	7,50	6,81	41,42	33,87	22,31%
					mW	mW	mW	mW	mW	

Data for 2.5 mm of 1.0 fF/um wire

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	3									
Supply (V)	1,1	MP3	0,492	0,361	18,87	3,32	3,27	25,46	25,72	-1,01%
Bus size	72	PDF	0,464	0,352	18,40	3,32	3,27	24,99	24,25	3,02%
Redundancy lines	9	JPG	0,488	0,359	18,77	3,32	3,27	25,35	25,51	-0,61%
Frequency (MHz)	**200**	TXT	0,327	0,31	16,20	3,32	3,27	22,79	17,09	33,34%
		WMV	0,488	0,358	18,71	3,32	3,27	25,30	25,51	-0,82%
		YUV-CIF	0,291	0,233	12,18	3,32	3,27	18,77	15,21	23,37%
		YUV-QCIF	0,311	0,249	13,02	3,32	3,27	19,60	16,26	20,58%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	3									
Supply (V)	1,1	MP3	0,492	0,361	37,74	6,95	6,53	51,22	51,44	-0,41%
Bus size	72	PDF	0,464	0,352	36,80	6,95	6,53	50,28	48,51	3,66%
Redundancy lines	9	JPG	0,488	0,359	37,53	6,95	6,53	51,02	51,02	0,00%
Frequency (MHz)	**400**	TXT	0,327	0,31	32,41	6,95	6,53	45,89	34,19	34,24%
		WMV	0,488	0,358	37,43	6,95	6,53	50,91	51,02	-0,21%
		YUV-CIF	0,291	0,233	24,36	6,95	6,53	37,84	30,42	24,39%
		YUV-QCIF	0,311	0,249	26,03	6,95	6,53	39,52	32,51	21,54%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	3									
Supply (V)	1,1	MP3	0,492	0,361	47,18	8,80	8,17	64,14	64,29	-0,24%
Bus size	72	PDF	0,464	0,352	46,00	8,80	8,17	62,97	60,64	3,84%
Redundancy lines	9	JPG	0,488	0,359	46,91	8,80	8,17	63,88	63,77	0,17%
Frequency (MHz)	**500**	TXT	0,327	0,31	40,51	8,80	8,17	57,48	42,73	34,51%
		WMV	0,488	0,358	46,78	8,80	8,17	63,75	63,77	-0,03%
		YUV-CIF	0,291	0,233	30,45	8,80	8,17	47,42	38,03	24,69%
		YUV-QCIF	0,311	0,249	32,54	8,80	8,17	49,51	40,64	21,81%
					mW	mW	mW	mW	mW	

Data for 3 mm of 1.0 fF/um wire

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	3,5									
Supply (V)	1,1	MP3	0,492	0,361	22,02	3,72	3,81	29,55	30,00	-1,52%
Bus size	72	PDF	0,464	0,352	21,47	3,72	3,81	29,00	28,30	2,48%
Redundancy lines	9	JPG	0,488	0,359	21,89	3,72	3,81	29,42	29,76	-1,13%
Frequency (MHz)	**200**	TXT	0,327	0,31	18,91	3,72	3,81	26,44	19,94	32,57%
		WMV	0,488	0,358	21,83	3,72	3,81	29,36	29,76	-1,33%
		YUV-CIF	0,291	0,233	14,21	3,72	3,81	21,74	17,75	22,51%
		YUV-QCIF	0,311	0,249	15,19	3,72	3,81	22,72	18,97	19,77%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	3,5									
Supply (V)	1,1	MP3	0,492	0,361	44,03	7,84	7,62	59,49	60,01	-0,86%
Bus size	72	PDF	0,464	0,352	42,93	7,84	7,62	58,40	56,59	3,19%
Redundancy lines	9	JPG	0,488	0,359	43,79	7,84	7,62	59,25	59,52	-0,46%
Frequency (MHz)	**400**	TXT	0,327	0,31	37,81	7,84	7,62	53,27	39,88	33,57%
		WMV	0,488	0,358	43,66	7,84	7,62	59,13	59,52	-0,66%
		YUV-CIF	0,291	0,233	28,42	7,84	7,62	43,88	35,49	23,64%
		YUV-QCIF	0,311	0,249	30,37	7,84	7,62	45,83	37,93	20,83%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	3,5									
Supply (V)	1,1	MP3	0,492	0,361	55,04	9,93	9,53	74,50	75,01	-0,68%
Bus size	72	PDF	0,464	0,352	53,67	9,93	9,53	73,12	70,74	3,37%
Redundancy lines	9	JPG	0,488	0,359	54,73	9,93	9,53	74,19	74,40	-0,28%
Frequency (MHz)	**500**	TXT	0,327	0,31	47,26	9,93	9,53	66,72	49,85	33,83%
		WMV	0,488	0,358	54,58	9,93	9,53	74,04	74,40	-0,49%
		YUV-CIF	0,291	0,233	35,52	9,93	9,53	54,98	44,37	23,93%
		YUV-QCIF	0,311	0,249	37,96	9,93	9,53	57,42	47,42	21,10%
					mW	mW	mW	mW	mW	

Data for 3.5 mm of 1.0 fF/um wire

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	5									
Supply (V)	1,1	MP3	0,492	0,361	31,45	5,03	5,45	41,93	42,86	-2,19%
Bus size	72	PDF	0,464	0,352	30,67	5,03	5,45	41,14	40,42	1,78%
Redundancy lines	9	JPG	0,488	0,359	31,28	5,03	5,45	41,75	42,51	-1,80%
Frequency (MHz)	**200**	TXT	0,327	0,31	27,01	5,03	5,45	37,48	28,49	31,57%
		WMV	0,488	0,358	31,19	5,03	5,45	41,66	42,51	-2,00%
		YUV-CIF	0,291	0,233	20,30	5,03	5,45	30,77	25,35	21,39%
		YUV-QCIF	0,311	0,249	21,69	5,03	5,45	32,17	27,09	18,73%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	5									
Supply (V)	1,1	MP3	0,492	0,361	62,90	10,28	10,89	84,07	85,73	-1,93%
Bus size	72	PDF	0,464	0,352	61,33	10,28	10,89	82,50	80,85	2,05%
Redundancy lines	9	JPG	0,488	0,359	62,55	10,28	10,89	83,72	85,03	-1,54%
Frequency (MHz)	**400**	TXT	0,327	0,31	54,01	10,28	10,89	75,18	56,98	31,96%
		WMV	0,488	0,358	62,38	10,28	10,89	83,55	85,03	-1,74%
		YUV-CIF	0,291	0,233	40,60	10,28	10,89	61,77	50,70	21,82%
		YUV-QCIF	0,311	0,249	43,39	10,28	10,89	64,56	54,19	19,13%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	5									
Supply (V)	1,1	MP3	0,492	0,361	78,63	13,26	13,61	105,50	107,16	-1,55%
Bus size	72	PDF	0,464	0,352	76,67	13,26	13,61	103,54	101,06	2,45%
Redundancy lines	9	JPG	0,488	0,359	78,19	13,26	13,61	105,06	106,29	-1,15%
Frequency (MHz)	**500**	TXT	0,327	0,31	67,52	13,26	13,61	94,39	71,22	32,53%
		WMV	0,488	0,358	77,97	13,26	13,61	104,84	106,29	-1,36%
		YUV-CIF	0,291	0,233	50,75	13,26	13,61	77,62	63,38	22,47%
		YUV-QCIF	0,311	0,249	54,23	13,26	13,61	81,10	67,74	19,74%
					mW	mW	mW	mW	mW	

Data for 5 mm of 1.0 fF/um wire

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	1,5									
Supply (V)	1,1	MP3	0,492	0,361	9,44	1,93	1,63	13,00	12,86	1,09%
Bus size	72	PDF	0,464	0,352	9,20	1,93	1,63	12,76	12,13	5,25%
Redundancy lines	9	JPG	0,488	0,359	9,38	1,93	1,63	12,95	12,75	1,51%
Frequency (MHz)	**200**	TXT	0,327	0,31	8,10	1,93	1,63	11,67	8,55	36,50%
		WMV	0,488	0,358	9,36	1,93	1,63	12,92	12,75	1,30%
		YUV-CIF	0,291	0,233	6,09	1,93	1,63	9,65	7,61	26,92%
		YUV-QCIF	0,311	0,249	6,51	1,93	1,63	10,07	8,13	23,90%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	1,5									
Supply (V)	1,1	MP3	0,492	0,361	18,87	4,13	3,27	26,27	25,72	2,14%
Bus size	72	PDF	0,464	0,352	18,40	4,13	3,27	25,80	24,25	6,36%
Redundancy lines	9	JPG	0,488	0,359	18,77	4,13	3,27	26,16	25,51	2,56%
Frequency (MHz)	**400**	TXT	0,327	0,31	16,20	4,13	3,27	23,60	17,09	38,08%
		WMV	0,488	0,358	18,71	4,13	3,27	26,11	25,51	2,36%
		YUV-CIF	0,291	0,233	12,18	4,13	3,27	19,58	15,21	28,70%
		YUV-QCIF	0,311	0,249	13,02	4,13	3,27	20,41	16,26	25,57%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	1,5									
Supply (V)	1,1	MP3	0,492	0,361	23,59	5,16	4,08	32,83	32,15	2,13%
Bus size	72	PDF	0,464	0,352	23,00	5,16	4,08	32,24	30,32	6,35%
Redundancy lines	9	JPG	0,488	0,359	23,46	5,16	4,08	32,70	31,89	2,56%
Frequency (MHz)	**500**	TXT	0,327	0,31	20,26	5,16	4,08	29,50	21,37	38,06%
		WMV	0,488	0,358	23,39	5,16	4,08	32,64	31,89	2,35%
		YUV-CIF	0,291	0,233	15,22	5,16	4,08	24,47	19,01	28,68%
		YUV-QCIF	0,311	0,249	16,27	5,16	4,08	25,51	20,32	25,55%
					mW	mW	mW	mW	mW	

Data for 1 mm of 1.5 fF/um wire

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	2,25									
Supply (V)	1,1	MP3	0,492	0,361	14,15	2,60	2,45	19,20	19,29	-0,44%
Bus size	72	PDF	0,464	0,352	13,80	2,60	2,45	18,85	18,19	3,62%
Redundancy lines	9	JPG	0,488	0,359	14,07	2,60	2,45	19,12	19,13	-0,04%
Frequency (MHz)	**200**	TXT	0,327	0,31	12,15	2,60	2,45	17,20	12,82	34,20%
		WMV	0,488	0,358	14,04	2,60	2,45	19,09	19,13	-0,24%
		YUV-CIF	0,291	0,233	9,13	2,60	2,45	14,18	11,41	24,34%
		YUV-QCIF	0,311	0,249	9,76	2,60	2,45	14,81	12,19	21,49%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	2,25									
Supply (V)	1,1	MP3	0,492	0,361	28,31	5,35	4,90	38,56	38,58	-0,05%
Bus size	72	PDF	0,464	0,352	27,60	5,35	4,90	37,85	36,38	4,04%
Redundancy lines	9	JPG	0,488	0,359	28,15	5,35	4,90	38,40	38,26	0,36%
Frequency (MHz)	**400**	TXT	0,327	0,31	24,31	5,35	4,90	34,56	25,64	34,78%
		WMV	0,488	0,358	28,07	5,35	4,90	38,32	38,26	0,15%
		YUV-CIF	0,291	0,233	18,27	5,35	4,90	28,52	22,82	24,99%
		YUV-QCIF	0,311	0,249	19,52	5,35	4,90	29,77	24,38	22,10%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	2,25									
Supply (V)	1,1	MP3	0,492	0,361	35,38	7,04	6,13	48,55	48,22	0,68%
Bus size	72	PDF	0,464	0,352	34,50	7,04	6,13	47,67	45,48	4,81%
Redundancy lines	9	JPG	0,488	0,359	35,19	7,04	6,13	48,35	47,83	1,09%
Frequency (MHz)	**500**	TXT	0,327	0,31	30,38	7,04	6,13	43,55	32,05	35,88%
		WMV	0,488	0,358	35,09	7,04	6,13	48,25	47,83	0,89%
		YUV-CIF	0,291	0,233	22,84	7,04	6,13	36,00	28,52	26,23%
		YUV-QCIF	0,311	0,249	24,40	7,04	6,13	37,57	30,48	23,26%
					mW	mW	mW	mW	mW	

Data for 1.5 mm of 1.5 fF/um wire

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	3									
Supply (V)	1,1	MP3	0,492	0,361	18,87	3,32	3,27	25,46	25,72	-1,01%
Bus size	72	PDF	0,464	0,352	18,40	3,32	3,27	24,99	24,25	3,02%
Redundancy lines	9	JPG	0,488	0,359	18,77	3,32	3,27	25,35	25,51	-0,61%
Frequency (MHz)	**200**	TXT	0,327	0,31	16,20	3,32	3,27	22,79	17,09	33,34%
		WMV	0,488	0,358	18,71	3,32	3,27	25,30	25,51	-0,82%
		YUV-CIF	0,291	0,233	12,18	3,32	3,27	18,77	15,21	23,37%
		YUV-QCIF	0,311	0,249	13,02	3,32	3,27	19,60	16,26	20,58%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	3									
Supply (V)	1,1	MP3	0,492	0,361	37,74	6,95	6,53	51,22	51,44	-0,41%
Bus size	72	PDF	0,464	0,352	36,80	6,95	6,53	50,28	48,51	3,66%
Redundancy lines	9	JPG	0,488	0,359	37,53	6,95	6,53	51,02	51,02	0,00%
Frequency (MHz)	**400**	TXT	0,327	0,31	32,41	6,95	6,53	45,89	34,19	34,24%
		WMV	0,488	0,358	37,43	6,95	6,53	50,91	51,02	-0,21%
		YUV-CIF	0,291	0,233	24,36	6,95	6,53	37,84	30,42	24,39%
		YUV-QCIF	0,311	0,249	26,03	6,95	6,53	39,52	32,51	21,54%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	3									
Supply (V)	1,1	MP3	0,492	0,361	47,18	8,80	8,17	64,14	64,29	-0,24%
Bus size	72	PDF	0,464	0,352	46,00	8,80	8,17	62,97	60,64	3,84%
Redundancy lines	9	JPG	0,488	0,359	46,91	8,80	8,17	63,88	63,77	0,17%
Frequency (MHz)	**500**	TXT	0,327	0,31	40,51	8,80	8,17	57,48	42,73	34,51%
		WMV	0,488	0,358	46,78	8,80	8,17	63,75	63,77	-0,03%
		YUV-CIF	0,291	0,233	30,45	8,80	8,17	47,42	38,03	24,69%
		YUV-QCIF	0,311	0,249	32,54	8,80	8,17	49,51	40,64	21,81%
					mW	mW	mW	mW	mW	

Data for 2 mm of 1.5 fF/um wire

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	3,75									
Supply (V)	1,1	MP3	0,492	0,361	23,59	3,88	4,08	31,55	32,15	-1,85%
Bus size	72	PDF	0,464	0,352	23,00	3,88	4,08	30,96	30,32	2,13%
Redundancy lines	9	JPG	0,488	0,359	23,46	3,88	4,08	31,42	31,89	-1,46%
Frequency (MHz)	**200**	TXT	0,327	0,31	20,26	3,88	4,08	28,22	21,37	32,07%
		WMV	0,488	0,358	23,39	3,88	4,08	31,36	31,89	-1,66%
		YUV-CIF	0,291	0,233	15,22	3,88	4,08	23,19	19,01	21,95%
		YUV-QCIF	0,311	0,249	16,27	3,88	4,08	24,23	20,32	19,25%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	3,75									
Supply (V)	1,1	MP3	0,492	0,361	47,18	8,08	8,17	63,42	64,29	-1,36%
Bus size	72	PDF	0,464	0,352	46,00	8,08	8,17	62,25	60,64	2,66%
Redundancy lines	9	JPG	0,488	0,359	46,91	8,08	8,17	63,16	63,77	-0,96%
Frequency (MHz)	**400**	TXT	0,327	0,31	40,51	8,08	8,17	56,76	42,73	32,82%
		WMV	0,488	0,358	46,78	8,08	8,17	63,03	63,77	-1,16%
		YUV-CIF	0,291	0,233	30,45	8,08	8,17	46,70	38,03	22,79%
		YUV-QCIF	0,311	0,249	32,54	8,08	8,17	48,79	40,64	20,04%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	3,75									
Supply (V)	1,1	MP3	0,492	0,361	58,97	10,25	10,21	79,43	80,37	-1,17%
Bus size	72	PDF	0,464	0,352	57,50	10,25	10,21	77,96	75,79	2,86%
Redundancy lines	9	JPG	0,488	0,359	58,64	10,25	10,21	79,10	79,71	-0,77%
Frequency (MHz)	**500**	TXT	0,327	0,31	50,64	10,25	10,21	71,10	53,42	33,10%
		WMV	0,488	0,358	58,48	10,25	10,21	78,94	79,71	-0,97%
		YUV-CIF	0,291	0,233	38,06	10,25	10,21	58,52	47,53	23,11%
		YUV-QCIF	0,311	0,249	40,67	10,25	10,21	61,13	50,80	20,34%
					mW	mW	mW	mW	mW	

Data for 2.5 mm of 1.5 fF/um wire

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	4,5									
Supply (V)	1,1	MP3	0,492	0,361	28,31	4,52	4,90	37,73	38,58	-2,21%
Bus size	72	PDF	0,464	0,352	27,60	4,52	4,90	37,02	36,38	1,76%
Redundancy lines	9	JPG	0,488	0,359	28,15	4,52	4,90	37,57	38,26	-1,81%
Frequency (MHz)	**200**	TXT	0,327	0,31	24,31	4,52	4,90	33,73	25,64	31,54%
		WMV	0,488	0,358	28,07	4,52	4,90	37,49	38,26	-2,02%
		YUV-CIF	0,291	0,233	18,27	4,52	4,90	27,69	22,82	21,36%
		YUV-QCIF	0,311	0,249	19,52	4,52	4,90	28,94	24,38	18,70%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	4,5									
Supply (V)	1,1	MP3	0,492	0,361	56,61	9,40	9,80	75,81	77,15	-1,74%
Bus size	72	PDF	0,464	0,352	55,20	9,40	9,80	74,40	72,76	2,25%
Redundancy lines	9	JPG	0,488	0,359	56,30	9,40	9,80	75,50	76,53	-1,34%
Frequency (MHz)	**400**	TXT	0,327	0,31	48,61	9,40	9,80	67,81	51,28	32,25%
		WMV	0,488	0,358	56,14	9,40	9,80	75,34	76,53	-1,55%
		YUV-CIF	0,291	0,233	36,54	9,40	9,80	55,74	45,63	22,15%
		YUV-QCIF	0,311	0,249	39,05	9,40	9,80	58,25	48,77	19,44%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	4,5									
Supply (V)	1,1	MP3	0,492	0,361	70,76	12,11	12,25	95,12	96,44	-1,37%
Bus size	72	PDF	0,464	0,352	69,00	12,11	12,25	93,36	90,95	2,65%
Redundancy lines	9	JPG	0,488	0,359	70,37	12,11	12,25	94,73	95,66	-0,97%
Frequency (MHz)	**500**	TXT	0,327	0,31	60,77	12,11	12,25	85,13	64,10	32,81%
		WMV	0,488	0,358	70,18	12,11	12,25	94,54	95,66	-1,17%
		YUV-CIF	0,291	0,233	45,67	12,11	12,25	70,03	57,04	22,78%
		YUV-QCIF	0,311	0,249	48,81	12,11	12,25	73,17	60,96	20,03%
					mW	mW	mW	mW	mW	

Data for 3 mm of 1.5 fF/um wire

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	5,25									
Supply (V)	1,1	MP3	0,492	0,361	33,02	5,36	5,72	44,10	45,01	-2,01%
Bus size	72	PDF	0,464	0,352	32,20	5,36	5,72	43,28	42,44	1,96%
Redundancy lines	9	JPG	0,488	0,359	32,84	5,36	5,72	43,92	44,64	-1,62%
Frequency (MHz)	**200**	TXT	0,327	0,31	28,36	5,36	5,72	39,43	29,91	31,83%
		WMV	0,488	0,358	32,75	5,36	5,72	43,83	44,64	-1,82%
		YUV-CIF	0,291	0,233	21,31	5,36	5,72	32,39	26,62	21,68%
		YUV-QCIF	0,311	0,249	22,78	5,36	5,72	33,85	28,45	19,00%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	5,25									
Supply (V)	1,1	MP3	0,492	0,361	66,05	10,83	11,43	88,31	90,01	-1,89%
Bus size	72	PDF	0,464	0,352	64,40	10,83	11,43	86,66	84,89	2,09%
Redundancy lines	9	JPG	0,488	0,359	65,68	10,83	11,43	87,94	89,28	-1,50%
Frequency (MHz)	**400**	TXT	0,327	0,31	56,72	10,83	11,43	78,98	59,83	32,02%
		WMV	0,488	0,358	65,50	10,83	11,43	87,76	89,28	-1,70%
		YUV-CIF	0,291	0,233	42,63	10,83	11,43	64,89	53,24	21,89%
		YUV-QCIF	0,311	0,249	45,56	10,83	11,43	67,82	56,90	19,19%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	5,25									
Supply (V)	1,1	MP3	0,492	0,361	82,56	13,60	14,29	110,45	112,52	-1,84%
Bus size	72	PDF	0,464	0,352	80,50	13,60	14,29	108,39	106,11	2,15%
Redundancy lines	9	JPG	0,488	0,359	82,10	13,60	14,29	109,99	111,60	-1,44%
Frequency (MHz)	**500**	TXT	0,327	0,31	70,89	13,60	14,29	98,79	74,78	32,10%
		WMV	0,488	0,358	81,87	13,60	14,29	109,76	111,60	-1,65%
		YUV-CIF	0,291	0,233	53,28	13,60	14,29	81,18	66,55	21,98%
		YUV-QCIF	0,311	0,249	56,94	13,60	14,29	84,84	71,12	19,28%
					mW	mW	mW	mW	mW	

Data for 3.5 mm of 1.5 fF/um wire

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	7,5									
Supply (V)	1,1	MP3	0,492	0,361	47,18	7,39	8,17	62,73	64,29	-2,43%
Bus size	72	PDF	0,464	0,352	46,00	7,39	8,17	61,56	60,64	1,52%
Redundancy lines	9	JPG	0,488	0,359	46,91	7,39	8,17	62,47	63,77	-2,04%
Frequency (MHz)	**200**	TXT	0,327	0,31	40,51	7,39	8,17	56,07	42,73	31,21%
		WMV	0,488	0,358	46,78	7,39	8,17	62,34	63,77	-2,24%
		YUV-CIF	0,291	0,233	30,45	7,39	8,17	46,01	38,03	20,98%
		YUV-QCIF	0,311	0,249	32,54	7,39	8,17	48,10	40,64	18,34%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	7,5									
Supply (V)	1,1	MP3	0,492	0,361	94,35	14,62	16,34	125,31	128,59	-2,55%
Bus size	72	PDF	0,464	0,352	92,00	14,62	16,34	122,95	121,27	1,39%
Redundancy lines	9	JPG	0,488	0,359	93,83	14,62	16,34	124,78	127,54	-2,16%
Frequency (MHz)	**400**	TXT	0,327	0,31	81,02	14,62	16,34	111,98	85,46	31,02%
		WMV	0,488	0,358	93,57	14,62	16,34	124,52	127,54	-2,37%
		YUV-CIF	0,291	0,233	60,90	14,62	16,34	91,85	76,06	20,77%
		YUV-QCIF	0,311	0,249	65,08	14,62	16,34	96,03	81,28	18,15%
					mW	mW	mW	mW	mW	

Tech (nm)	65	Data	Reference SW	Switching activity	Bus Power	Overhead	Redundancy	Total Power	Reference	Improvement
Load (pF)	7,5									
Supply (V)	1,1	MP3	0,492	0,361	117,94	18,73	20,42	157,09	160,74	-2,27%
Bus size	72	PDF	0,464	0,352	115,00	18,73	20,42	154,15	151,59	1,69%
Redundancy lines	9	JPG	0,488	0,359	117,29	18,73	20,42	156,43	159,43	-1,88%
Frequency (MHz)	**500**	TXT	0,327	0,31	101,28	18,73	20,42	140,43	106,83	31,45%
		WMV	0,488	0,358	116,96	18,73	20,42	156,11	159,43	-2,08%
		YUV-CIF	0,291	0,233	76,12	18,73	20,42	115,27	95,07	21,25%
		YUV-QCIF	0,311	0,249	81,35	18,73	20,42	120,50	101,60	18,60%
					mW	mW	mW	mW	mW	

Data for 5 mm of 1.5 fF/um wire

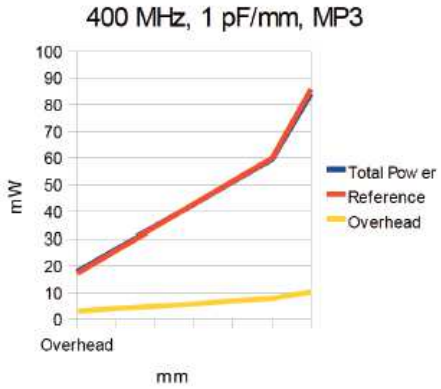
A graphic overview for the MP3 data format at 400 – 500 MHz is shown below:

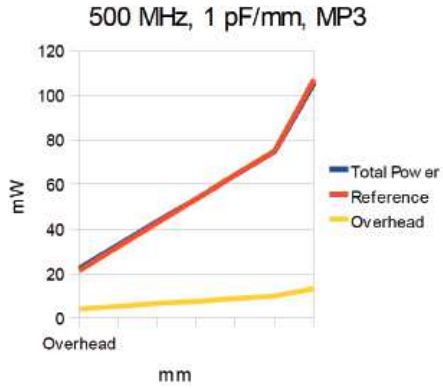
400 MHz

mm	Overhead	Reference	Total Power	Improvement
1	3,1	17,15	17,86	4,16%
1,5	4,13	25,72	26,27	2,14%
2	4,9	34,29	34,42	0,37%
2,5	5,78	42,86	42,68	-0,44%
3	6,95	51,44	51,22	-0,41%
3,5	7,84	60,01	59,49	-0,86%
5	10,28	85,73	84,07	-1,93%

500 MHz

mm	Overhead	Reference	Total Power	Improvement
1	4,04	21,43	22,49	4,93%
1,5	5,16	32,15	32,83	2,13%
2	6,54	42,86	43,44	1,34%
2,5	7,5	53,58	53,62	0,08%
3	8,8	64,30	64,14	-0,24%
3,5	9,93	75,01	74,80	-0,68%
5	13,26	107,16	105,50	-1,55%



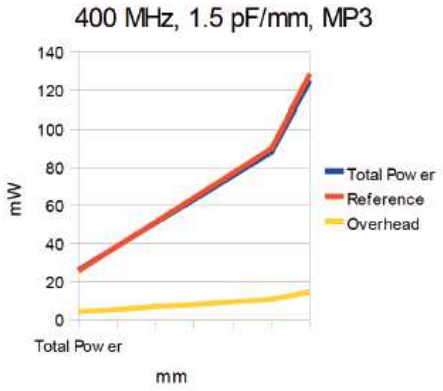


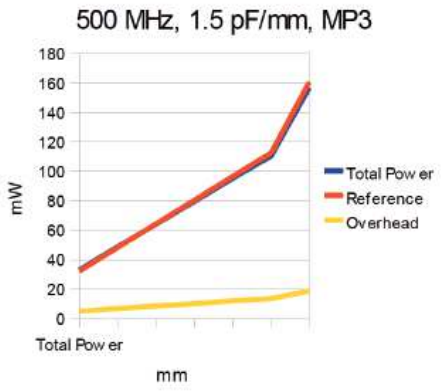
400 MHz

mm	Overhead	Reference	Total Power	Improvement
1	4,13	25,72	26,27	2,14%
1,5	5,35	38,58	38,56	-0,05%
2	6,95	51,44	51,22	-0,41%
2,5	8,08	64,30	63,42	-1,36%
3	9,4	77,15	75,81	-1,74%
3,5	10,83	90,01	88,31	-1,89%
5	14,62	128,59	125,31	-2,55%

500 MHz

mm	Overhead	Reference	Total Power	Improvement
1	5,16	32,15	32,83	2,13%
1,5	7,04	48,22	48,55	0,68%
2	8,8	64,30	64,14	-0,24%
2,5	10,25	80,37	79,43	-1,17%
3	12,11	96,44	95,12	-1,37%
3,5	13,6	112,52	110,45	-1,84%
5	18,73	160,74	157,09	-2,27%

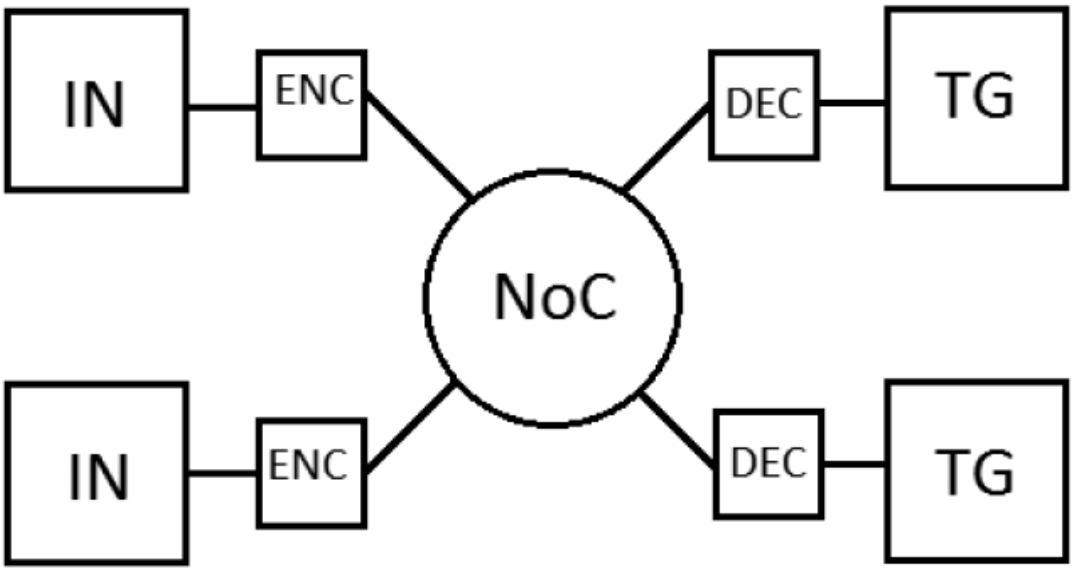




7. Power saving in NoCs

The presented data show that Segmented Bus Inverter outperformed the other analyzed techniques in terms of effective power-saving.
According to this, use for System-in-Package (SiP) wiring is possible.

Anyway, the effectiveness of such technique for fully-integrated single-chip devices was analyzed only for point-to-point connection.
In a network-on-chip it corresponds to a router-to-router connection, so further analysis is required for an end-to-end use (which means IP-to-IP communication).
In this context, global-network switching activity reduction is expected to provide a far larger improvement in power-saving, because with a higher number of devices involved, the dynamic power consumption of the encoder-decoder couple would become far less relevant than on single-link communication.
A sample architecture, with only 2 initiators and 2 targets connected by a single-node NoC, making use of two encoder-decoder couples is partially described by the data below.



Evaluation data of the presented techniques for full end-to-end STNoC® use is undergoing further development and cannot be disclosed due to industrial policy.

ws_AXI_STBus_2x2	200 MHz	65 nm		Module load = 0.5 pF			
	Reference SW	Reduced SW	Overhead	Network Power	Total Power	Reference Power	Improvement
MP3	0,492	0,361	2,06	730,42	732,48	730,66	0,25%
PDF	0,464	0,352	2,06	730,38	732,44	730,77	0,23%
JPG	0,488	0,359	2,06	730,40	732,46	730,77	0,23%
TXT	0,327	0,31	2,06	730,21	732,27	730,35	0,26%
WMV	0,488	0,358	2,06	730,39	732,45	730,77	0,23%
YUV-CIF	0,291	0,233	2,06	729,97	732,03	730,16	0,26%
YUV-QCIF	0,311	0,249	2,06	729,97	732,03	730,22	0,25%
			mW	mW	mW	mW	

Node-node distance = 1 mm Load = 1.5 fF/um
Link load = 1.5 pF

ws_AXI_STBus_2x2	200 MHz	65 nm		Module load = 0.5 pF			
	Reference SW	Reduced SW	Overhead	Network Power	Total Power	Reference Power	Improvement
MP3	0,492	0,361	2,06	731,93	733,99	733,07	0,13%
PDF	0,464	0,352	2,06	731,86	733,92	733,15	0,11%
JPG	0,488	0,359	2,06	731,93	733,99	733,09	0,12%
TXT	0,327	0,31	2,06	731,46	733,52	731,63	0,26%
WMV	0,488	0,358	2,06	731,93	733,99	733,09	0,12%
YUV-CIF	0,291	0,233	2,06	730,72	732,78	731,27	0,21%
YUV-QCIF	0,311	0,249	2,06	730,86	732,92	731,46	0,20%
			mW	mW	mW	mW	

Node-node distance = 2 mm Load = 1.5 fF/um
Link load = 3 pF

ws_AXI_STBus_2x2	200 MHz	65 nm		Module load = 0.5 pF			
	Reference SW	Reduced SW	Overhead	Network Power	Total Power	Reference Power	Improvement
MP3	0,492	0,361	2,06	731,93	733,99	733,07	0,13%
PDF	0,464	0,352	2,06	731,86	733,92	733,15	0,11%
JPG	0,488	0,359	2,06	731,93	733,99	733,09	0,12%
TXT	0,327	0,31	2,06	731,46	733,52	731,63	0,26%
WMV	0,488	0,358	2,06	731,93	733,99	733,09	0,12%
YUV-CIF	0,291	0,233	2,06	730,72	732,78	731,27	0,21%
YUV-QCIF	0,311	0,249	2,06	730,86	732,92	731,46	0,20%
			mW	mW	mW	mW	

Node-node distance = 3 mm Load = 1.5 fF/um
Link load = 4.5 pF

ws_AXI_STBus_2x2	200 MHz	40 nm		Module load = 0.5 pF			
	Reference SW	Reduced SW	Overhead	Network Power	Total Power	Reference Power	Improvement
MP3	0,492	0,361	1,56	17,06	18,62	17,75	4,90%
PDF	0,464	0,352	1,56	17,02	18,58	17,61	5,51%
JPG	0,488	0,359	1,56	17,05	18,61	17,73	4,96%
TXT	0,327	0,31	1,56	16,83	18,39	16,9	8,82%
WMV	0,488	0,358	1,56	17,05	18,61	17,73	4,96%
YUV-CIF	0,291	0,233	1,56	16,51	18,07	16,75	7,88%
YUV-QCIF	0,311	0,249	1,56	16,57	18,13	16,83	7,72%
			mW	mW	mW	mW	

Node-node distance = 1 mm Load = 1 fF/um
Link load = 1 pF

ws_AXI_STBus_2x2	200 MHz	40 nm		Module load = 0.5 pF			
	Reference SW	Reduced SW	Overhead	Network Power	Total Power	Reference Power	Improvement
MP3	0,492	0,361	1,56	17,08	18,64	17,75	5,01%
PDF	0,464	0,352	1,56	17,04	18,6	17,63	5,50%
JPG	0,488	0,359	1,56	17,07	18,63	17,75	4,96%
TXT	0,327	0,31	1,56	16,84	18,4	16,91	8,81%
WMV	0,488	0,358	1,56	17,07	18,63	17,75	4,96%
YUV-CIF	0,291	0,233	1,56	16,51	18,07	16,75	7,88%
YUV-QCIF	0,311	0,249	1,56	16,57	18,13	16,84	7,66%
			mW	mW	mW	mW	

Node-node distance = 2 mm Load = 1 fF/um
Link load = 2 pF

ws_AXI_STBus_2x2	200 MHz	32 nm		Module load = 0.5 pF			
	Reference SW	Reduced SW	Overhead	Network Power	Total Power	Reference Power	Improvement
MP3	0,492	0,361	1,24	23,14	24,38	23,32	4,55%
PDF	0,464	0,352	1,24	23,13	24,37	23,28	4,68%
JPG	0,488	0,359	1,24	23,14	24,38	23,32	4,55%
TXT	0,327	0,31	1,24	23,08	24,32	23,1	5,28%
WMV	0,488	0,358	1,24	23,14	24,38	23,32	4,55%
YUV-CIF	0,291	0,233	1,24	22,98	24,22	23,05	5,08%
YUV-QCIF	0,311	0,249	1,24	23	24,24	23,08	5,03%
			mW	mW	mW	mW	

Node-node distance = 1 mm Load = 0.5 fF/um
Link load = 0.5 pF

ws_AXI_STBus_2x2	200 MHz	32 nm		Module load = 0.5 pF			
	Reference SW	Reduced SW	Overhead	Network Power	Total Power	Reference Power	Improvement
MP3	0,492	0,361	1,24	23,15	24,39	23,32	4,59%
PDF	0,464	0,352	1,24	23,13	24,37	23,28	4,68%
JPG	0,488	0,359	1,24	23,15	24,39	23,33	4,54%
TXT	0,327	0,31	1,24	23,08	24,32	23,1	5,28%
WMV	0,488	0,358	1,24	23,14	24,38	23,33	4,50%
YUV-CIF	0,291	0,233	1,24	22,99	24,23	23,05	5,12%
YUV-QCIF	0,311	0,249	1,24	23,01	24,25	23,08	5,07%
			mW	mW	mW	mW	

Node-node distance = 2 mm Load = 0.5 fF/um
Link load = 1 pF

8. Error detection and correction: encoding techniques to reduce Bit Error Rate

Layered architectures in networks-on-chip require upper levels to be provided an abstraction of the physical link into an ideal transmission channel. This is one of the tasks of the data link layer.

In general, data transmission can be affected by errors, which in digital electronic sense are wrong bit values which randomly occur. Static CMOS, though being regarded as a set of noise-resistant technologies, is still affected by channel noise and thus can be subject to errors. Important causes of these errors include the limited noise margin of the gates, however high it may be, cross-talk from integrated communication systems, interference from neighbour microwave devices and many others.

End-to-end communication is verified by the hardware modules which implement one or more techniques of error detection and correction. These techniques have been widely explored in the field of mathematics, informatics and engineering for long time[9], and particularly in the context of telecommunication for computer networks[19].

This chapter presents some error detection and correction techniques from the point of view of hardware implementation in modern NoCs' data link.

1. Overview of traditional coding theory

Error detection and correction (EDC) is the field of coding theory which focuses on enabling reliable delivery of digital data over unreliable communication channels.

- **Error Detectors** – techniques which detect (but not correct) errors.

- **Error Correctors** – techniques which detect errors and reconstruct the original error-free data-format.

Error correction can be performed in two main ways:

- **Automatic Repeat Request (ARQ) / Backward Error Correction (BEC)** – the canonical way to ensure reliability is to inform the source through an acknowledgement and ask for data repetition in case of errors. Retransmission is asked until the data are properly received.

- **Forward Error Correction (FEC)** – the source encodes the message and the destination is able not only to determine whether or not an error occured, but also to reconstruct the original data (or what is deemed the “most likely” original data) on its own.

ARQ and FEC can be combined into **Hybrid Automatic Repeat Request (HARQ)** techniques, which is used when major errors are correct via ARQ techniques while minor guessing is performed by the target.

In general, EDC schemes consist of adding some *redundancy* (extra data) to the original message. This additional information is used by the target to check the received data.

Common techniques in the fields of informatics and telecommunication are mostly included in the following code families:

- **Repetition codes –** this simple ARQ scheme consists of transmitting the data a certain number of times. The target can guess whether the reiceved data are correct by confrontation and ask for retransmission if it is needed. Repetition codes are not very efficient, as they require an extremely large redundancy.
For example, transmitting 4 bits (useful data) 3 times requires 12 bits; redundancy is then 8 bit, which is 200% the useful data and 67% of the whole message.

- **Hamming codes**[19] – this technique makes use of *perfect codes*, which are codes that exactly match the theoretical upper bound on the number of distinct code words for a given number of bits. Adding some extra bits in key positions to the original message allows for error correction.

- **Checksum** – a message is constructed into codewords of known size and a special value, called checksum, is obtained as the modular arithmetic sum of a group of words. The checksum is then confronted to a reference, according to the specific algorithm.
Parity Word, Two's complement, Fletcher's Checksum, Adler-32 are widely used checksum algorithms.

- **Cyclic Redundancy Checks (CRC)**[9] – this error-detecting technique is well suited to detect burst errors and is widely used in Ethernet protocols. Its computation resembles a polynomial long division operation in which the quotient is discarded and the remainder becomes the result, but polynomial coefficient are calculated according to the carry-less arithmetic of a mathematical finite field. In this operation, the divisor is called *generator polynomial*. Different CRCs are defined according to the chosen generator.

- **Hash functions** – cryptographic hash functions allow the target to determine mismatches in the received message, through an autentication code, sometimes referred as digital fingerprint, hash value or checksum.

- **Convolutional codes** – the Error Correcting Codes (ECC) which are processed on a bit-by-bit basis; decoding of such codes is usually performed by the Viterbi decoder[20].

- **Block codes** – the ECCs which are processed on a block-by-block basis; Hamming codes can be considered part of this family, together with Repetition codes, Multi-dimensional Bit-Parity Checks, Reed-Solomon codes (a CRC subset, widely used in optical disks, DSL and WiMAX), Turbo codes and Low-Density Parity-Checks (LDPC).

2. Error detection and correction in hardware

In hardware, soft errors[24] (also referred to as single-event upsets) generally affect storage elements, such as memory, latches and registers, affecting the stored charge values, and subsequently the logic state of bits.
As technologies scale down, the noise margin decreases and a number of factors become relevant in their contribution to soft errors.

The most relevant ones are:

- **Neutron radiations** - they interfere with charges held within sensitive nodes in the circuit.

- **Particle collisions** – these phenomena are more and more likely to determine a critical modification in the stored charge values as the minimum feature size shrinks.

Manufacturers are increasingly taking soft error rates (SER) into serious account: they can determine increased Bit Error Rate in high-density memories and system-vulnerability to unpredictable malfunctions. Some improvements and precautions have been proposed in the manufacting process, i.e. the use of expensive silicon-on-insulator (SOI) substrates, trench capacitors and/or special single-transistor architectures to reduce the occurence of particle collisions.

Apart from the transistor-level point of view, some solutions can also be provided by hardware design at system level, taking advantage from the fact that, as of today, soft errors rates are still moderate and single-bit errors represent the most likely scenario. For example, software exceptions are implemented in some tightly-coupled memories (TCM) to perform complete system resets, while parity checks (see below) are already used for cache instructions, so that the detection of an error triggers a low-end flush/refresh of the pipeline. Hamming codes have often been proposed to provide protection for tags and other vulnerable data fields, but complete and multi-bit correction mechanisms pose a cost in terms of complexity, area and performance which is often hard to sustain.

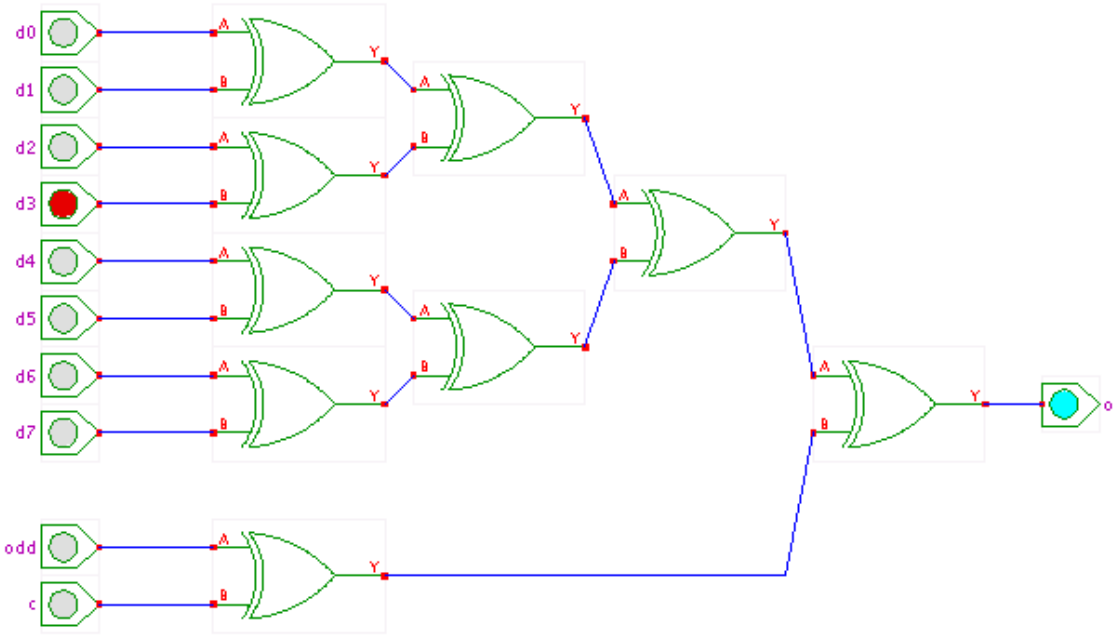
Indeed, the vast majority of the traditional techniques are designed for software implementation and mathematical research: they are usually well suited for low-level programming, but their logics are far too abstract and complex to be easily computed with the limited resources of the data link layer of a network-on-chip. They simply cannot comply to the strict requirements of high speed, moderate area occupation and low power-consumption which are required in such application.

3. Bit parity check in hardware

Bit Parity Check[19] is a simple 1-detector ARQ (*Automatic ReQuest*) technique.
Even parity is a special case of a Cyclic Redundancy Check (CRC)[9], where the 1-bit CRC is generated by the polynomial $x+1$.

In encoding phase, a single check line is added to the original phyt to mark whether the number of 1 in the phyt is odd or even. In decoding phase, the number of 1 in the phyt is counted again to check the correctness of the phyt. Only when the parity bit is coherent with the input lines, the phyt is considered valid.

7 bits of data (number of 1s)	8 bits including parity	
	even	odd
0000000 (0)	**0**0000000	**1**0000000
1010001 (3)	**1**1010001	**0**1010001
1101001 (4)	**0**1101001	**1**1101001
1111111 (7)	**1**1111111	**0**1111111



An example of 8-bit parity generator

```
ARCHITECTURE rtl OF parity IS

        SIGNAL chain:        STD_LOGIC_VECTOR(A DOWNTO 0);

BEGIN

        chain(A) = '0';
        FOR i IN A-1 DOWNTO 0 GENERATE
                chain(i) <= chain(i+1) XOR in0(i);
        END GENERATE;

        out0 <= chain(0);

END rtl;
```


```
ARCHITECTURE rtl OF parity IS

        SIGNAL chain:        STD_LOGIC_VECTOR(A DOWNTO 0);

BEGIN

        chain(A) = '0';
        FOR i IN A-1 DOWNTO 0 GENERATE
                chain(i) <= chain(i+1) XOR in0(i);
        END GENERATE;

        out0 <= chain(0);

END rtl;
```


Sample VHDL architecture of parity generator with generic number of bits A

It can be observed that an even number of errors in the same phyt brings to a non-detected error. This technique can detect (but not correct) an odd number of errors per phyt, thus it can be considered suitable only for single-error protocols.
Single-error detectors can be useful in NoCs, because of their simple logic (small area overhead and limited power consumption) and fast execution.

The table below shows synthesis results of a single-block 77-bit version and the equivalent 8-bit segmented (10 modules for a total of 80 bits).
Segmented version is obtained in the same way of power modules, and is expected to reduce critical paths: propagation delay of smaller modules is significantly reduced at the cost of further redundancy lines.

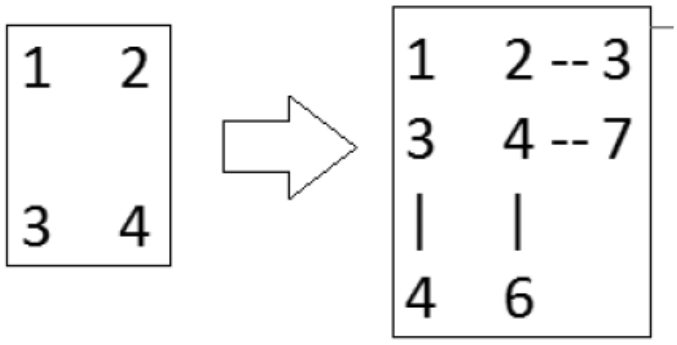
Bus size	DSM Technology	Clock limit*	Power overhead**	Area overhead	Redundancy
77	65 nm	633 MHz	1.82 mW	2866 standard cells	1 parity line
77	40 nm	750 MHz	1.46 mW	1664 standard cells	1 parity line
77	32 nm	867 MHz	1.34 mW	948 standard cells	1 parity line
8 x 10	65 nm	900 MHz	3.06 mW	3110 standard cells	10 parity line
8 x 10	40 nm	1033 MHz	2.48 mW	2190 standard cells	10 parity line
8 x 10	32 nm	1200 MHz	2.30 mW	1120 standard cells	10 parity line

* assuming input delay = 15% clock period, output delay = 10% clock period
** comprehensive of dynamic and static power consumption at the maximum working frequency (thus values are not directly comparable)

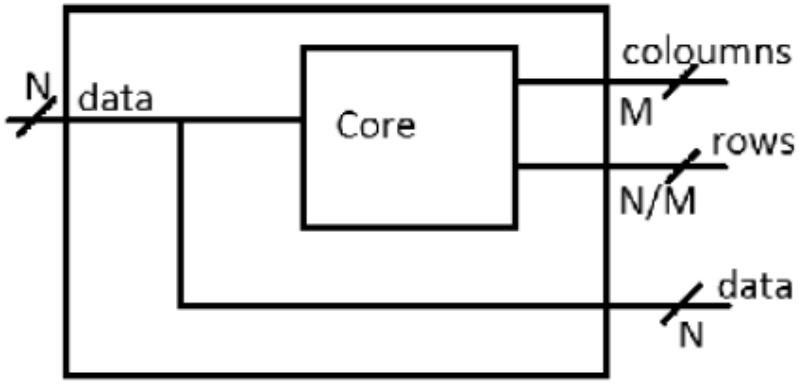
4. Multi-dimensional bit parity check in hardware

Multi-dimensional Bit Parity Check is a 1-corrector FEC (*Forward Error Correction*) technique. Traditional FEC techniques, such as *Hamming Distance Check*[9] and *Reed-Solomon Algorithm*[9], are not suitable for hardware implementation, due to their complexity (area, power and critical path would not be acceptable). Multi-Dimensional Bit Parity Check is usually discarded in the field of telecommunication, as it requires more redundancy than the other common techniques. In the context of electronics, however, this technique is far lighter to implement.

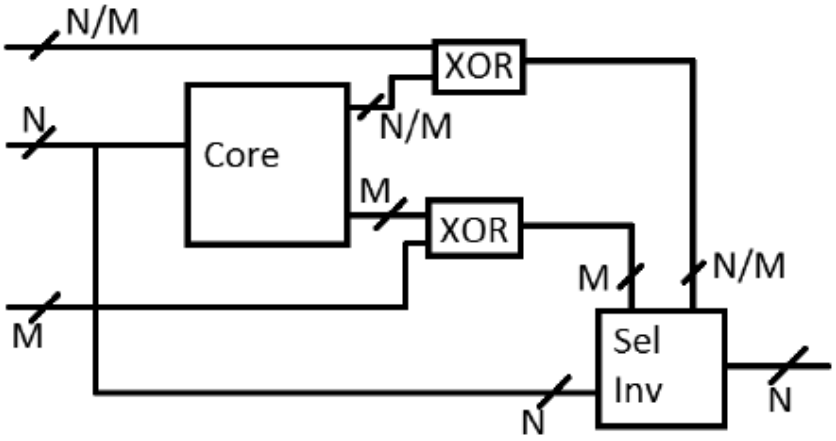
In the encoder, the original phyt is redistributed in a 2D matrix and parity checks are performed for each row and for each coloumn. The phyt is then transmitted with the row and coloumn parity check (which then become redundancy lines), which are verified by the decoder. If a bit in the phyt is affected by an error, then both its row and coloumn parity checks will provide an incoherence. A conditional inverter is instructed to invert only the bit whose parity checks are incoherent, thus correcting the error.



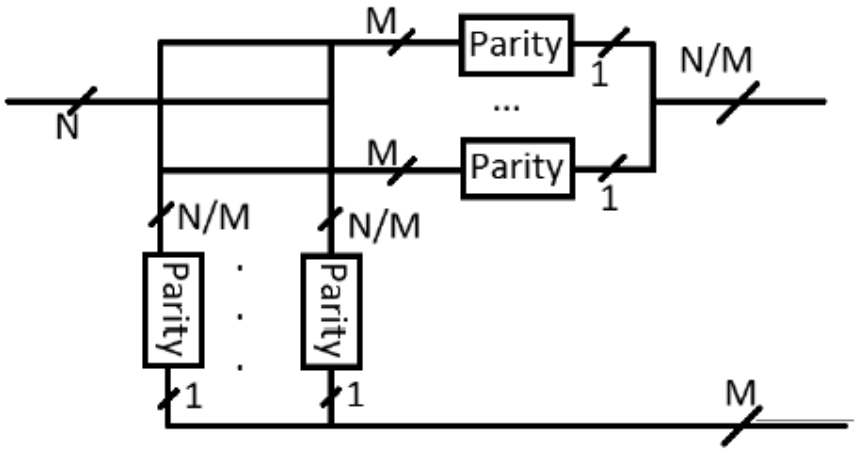
Encoder working principle



Encoder scheme
minimum redundancy is obtained with $M_{opt} = \sqrt{N}$



Decoder scheme
"Sel Inv" block inverts the bit whose row and coloumn are flagged wrong by the "Core" block



Core scheme

The described technique works only for single-error protocols: if two errors occure in the same phyt, then up to four bits are inverted, but only two of them were wrong. A multi-dimensional matrix can be used to correct a greater number of errors. In general, a Q-dimensional parity scheme can correct up to Q/2 errors.

Error-correctors require, in general, more redundancy bits and more complex logic than error-detectors.

Version	DSM Technology	Clock limit*	Power overhead**	Area overhead	Redundancy
72-bit single-block	65 nm	633 MHz	2.74 mW	3774 standard cells	17 parity lines
72-bit single-block	40 nm	833 MHz	2.80 mW	2590 standard cells	17 parity lines
72-bit single-block	32 nm	967 MHz	2.44 mW	1265 standard cells	17 parity lines

* assuming input delay = 15% clock period, output delay = 10% clock period
** comprehensive of dynamic and static power consumption at the maximum working frequency (thus values are not directly comparable)

9. Experimental data and future development

The activity described in this document aimed at the implementation of power-saving modules and error-correctors for on-chip and off-chip communication networks.

The main focus has been given to the topic of power-saving, through the analysis of various encoding techniques to provide reduction in power consumption, both for single-link and full-network cases of study.

Hardware-module techniques to reduce the Bit Error Rate and to provide more reliable communication for error detection and correction have been discussed as well.

Future developments for this work are largely possible.

The presented power-saving techniques can be re-applied in other electronic sub-systems, while similar evaluations can be performed on different on-chip and off-chip networks, and many design optimizations are possible when considering the data link layer as a comprehensive hardware system.

More efficient encoding techniques to reduce power consumption and BER are mainstream academic issues still undergoing relevant work and development by the scientific community.

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