Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Generic DDCM compatible with plasmonics-based PHY

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Executive Summary

This document describes the result of the design activity based on the functional specification of a generic Dual Die Communication Module exploiting a plasmonics-based PHY as physical layer (deliverable D5.4).

Change Records

Version	Date	Changes	Author
0.1 (draft)	2013-11-05	Start	Alberto Scandurra, Valentina Cernuto
1 (submission)	2014-01-31	Final version	Alberto Scandurra, Valentina Cernuto

1. *Contents*

2. Introduction

The **Dual Die Communication Module** (abbreviated **DDCM**) is the building-block responsible for the interconnection of different dice within a so called Network in Package (NiP), the communication system enabling inter dice data transmission in the context of Systems in Package (SiP) technology.

According to a widely used approach, the DDCM is considered composed of two main building blocks:

- the DDCM **controller**, responsible for managing incoming/outgoing STNoC traffic and IDN segments, generating them through STNoC flits encapsulation and preparing them to be sent to the PHY transmitter, as well as collecting them from the PHY receiver;
- the DDCM **PHY**, responsible for transmitting output phyts across the physical link and collecting inputs phyts from the physical link.

The next figure shows the DDCM structure in terms of top level building-blocks.

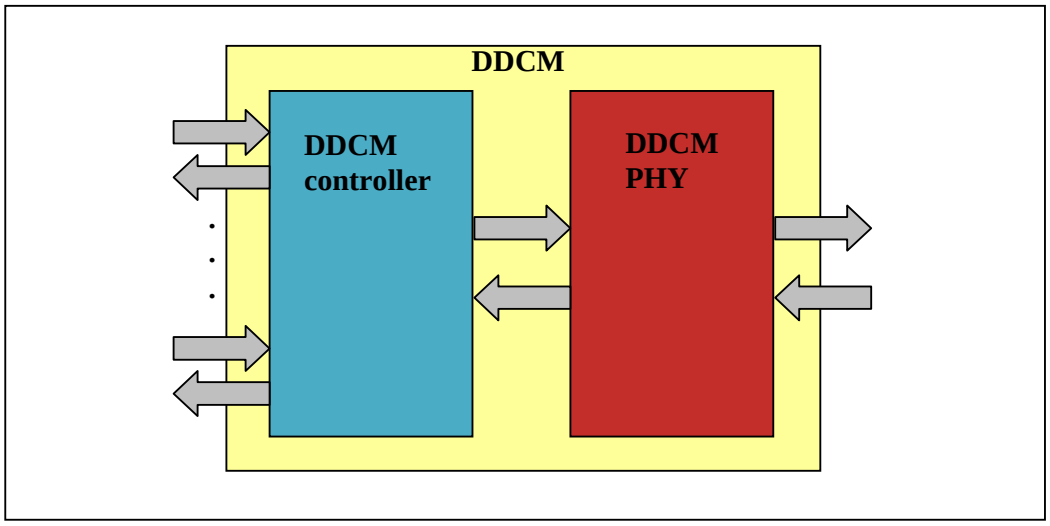

Figure 1-1: DDCM top level structure

Compared to the DDCM module with electrical PHY, described in deliverable D5.2 (DDCM specification document), this module exploits a plasmonics-based PHY, composed of plasmonic emitters and detectors, managed by a proper PHY adapter, a dedicated DDCM building-block converting the digital (CMOS) signals into analog signals able to interact with the plasmonic components.

A detailed description of the DDCM parameters, interfaces and registers can be found in deliverable D5.4 (Generic DDCM compatible with plasmonics-based PHY specification document).

3. Architecture

As shown in figure 2.1, the DDCM top level in each die consists of a transmitter (DDCM Tx) and a receiver (DDCM Rx).
In such a figure it's possible to see the two information flows supported by a complete DDCM architecture, i.e.

- requests from STNoC/STBus/AMBA-AXI initiators in chip 1 to STNoC/STBus/AMBA-AXI targets in chip 2, responses from STNoC/STBus/AMBA-AXI targets in chip 2 to STNoC/STBus/AMBA-AXI initiators in chip 1, virtual wires from chip 1 to chip 2 (continuous lines);
- requests from STNoC/STBus/AMBA-AXI initiators in chip 2 to STNoC/STBus/AMBA-AXI targets in chip 1, responses from STNoC/STBus/AMBA-AXI targets in chip 1 to STNoC/STBus/AMBA-AXI initiators in chip 2, virtual wires from chip 2 to chip 1 (dotted lines).

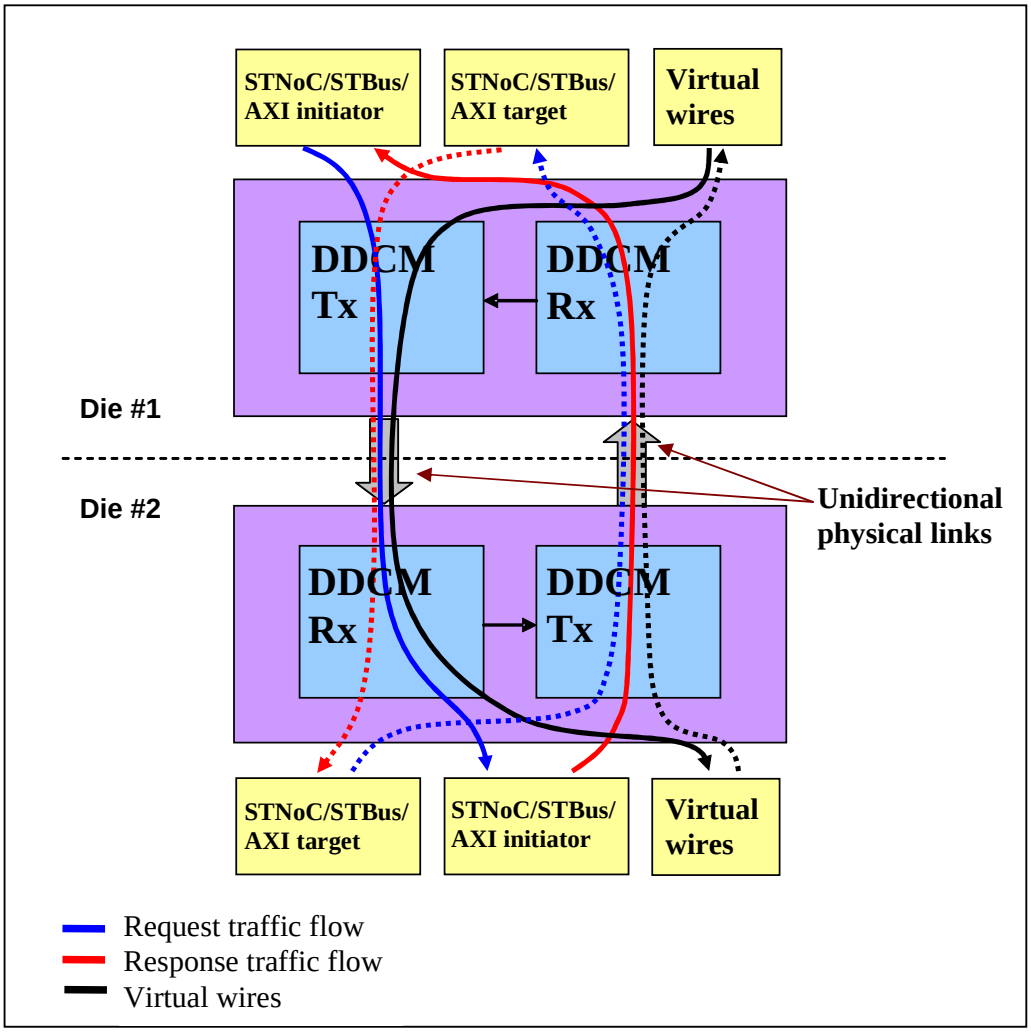

Figure 2-1: DDCM top level architecture and information flow

The DDCM transmitter (DDCM Tx) is responsible for

- receiving requests from STNoC/STBus/AMBA-AXI initiators in the same die and sending them to STNoC/STBus/AMBA-AXI targets in the other die;

- receiving responses from STNoC/STBus/AMBA-AXI targets in the same die and sending them to STNoC/STBus/AMBA-AXI initiators in the other die;
- sampling ancillary signals (virtual wires) generated in the same die at a specified rate and sending samples to the other die.

The DDCM receiver (DDCM Rx) is responsible for

- receiving requests from STNoC/STBus/AMBA-AXI initiators in the other die and sending them to STNoC/STBus/AMBA-AXI targets in the same die;
- receiving responses from STNoC/STBus/AMBA-AXI targets in the other die and sending them to STNoC/STBus/AMBA-AXI initiators in the same die;
- receiving ancillary signals samples generated in the other die and sending them to the proper destination in the same die.

Figure 2-2 shows a full architectural view of an DDCM, highlighting the separation between an DDCM transmitter and an DDCM receiver.

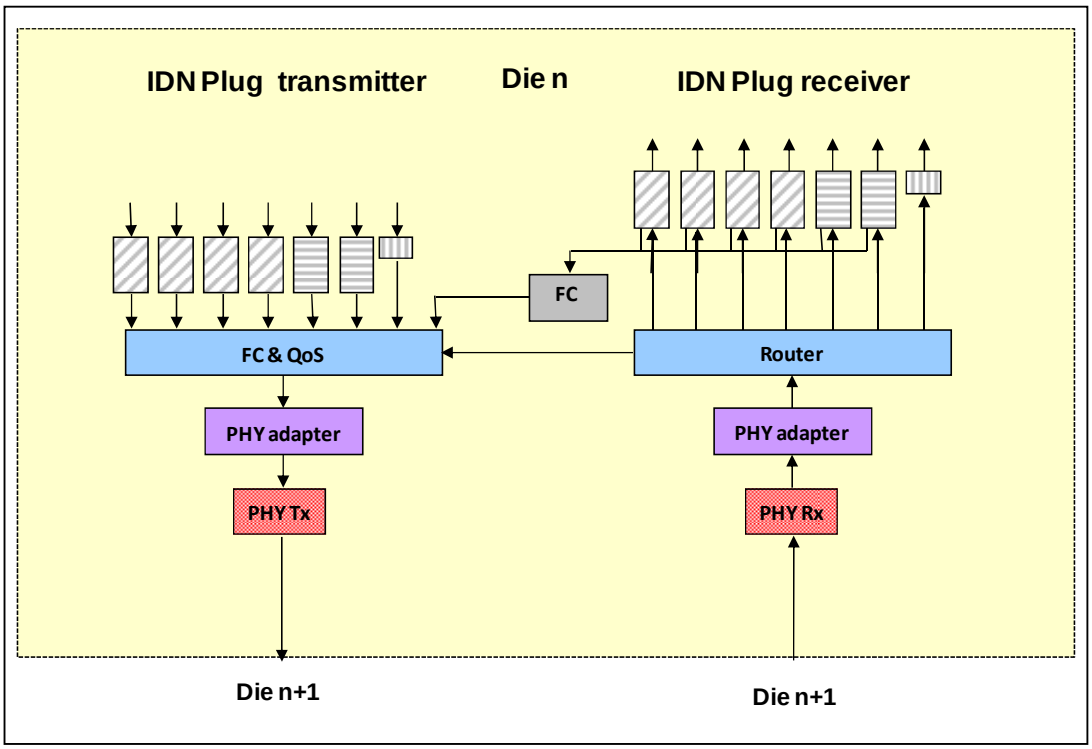

Figure 2-2: DDCM detailed architecture

Figure 2-3 shows the architecture of the DDCM highlighting the connections with initiators and targets across an STNoC interconnect. In this picture it's possible to see clearly how request and response traffic streams flow.

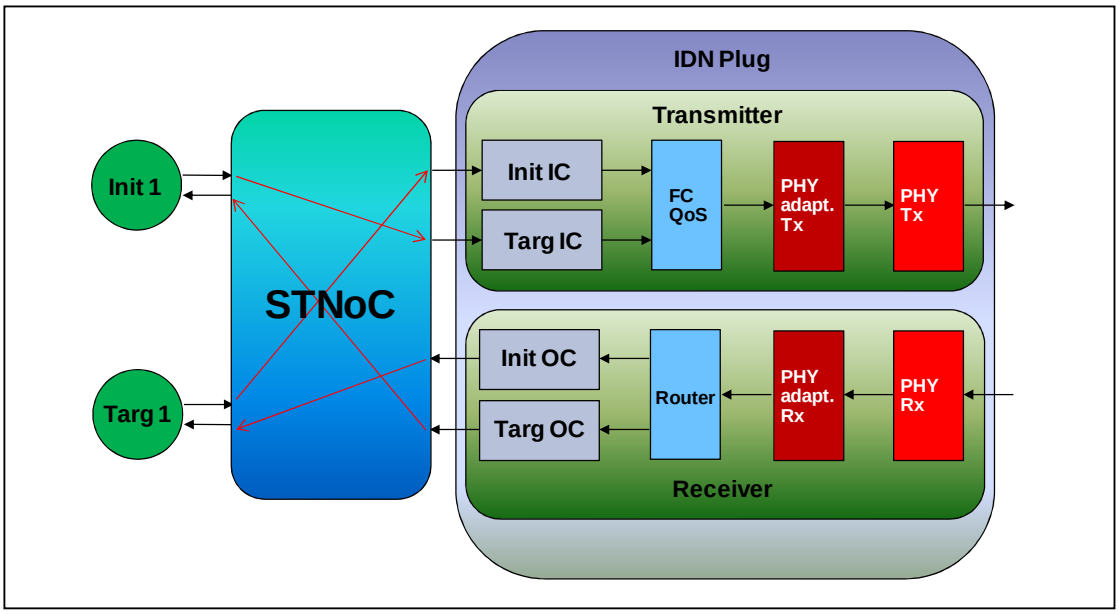

Figure 2-3: DDCM detailed architecture highlighting traffic streams flows

Figure 2-4 shows the connection and the traffic streams flows between two dice, highlighting the two DDCMs architectures and their crossing. Specifically, the orange line represents the request traffic stream flowring from initiator 1 in die #1 towards target 2 in die #2, while the yellow line represents the response traffic stream flowing from target 2 in die #2 toward initiator 1 in die #1.

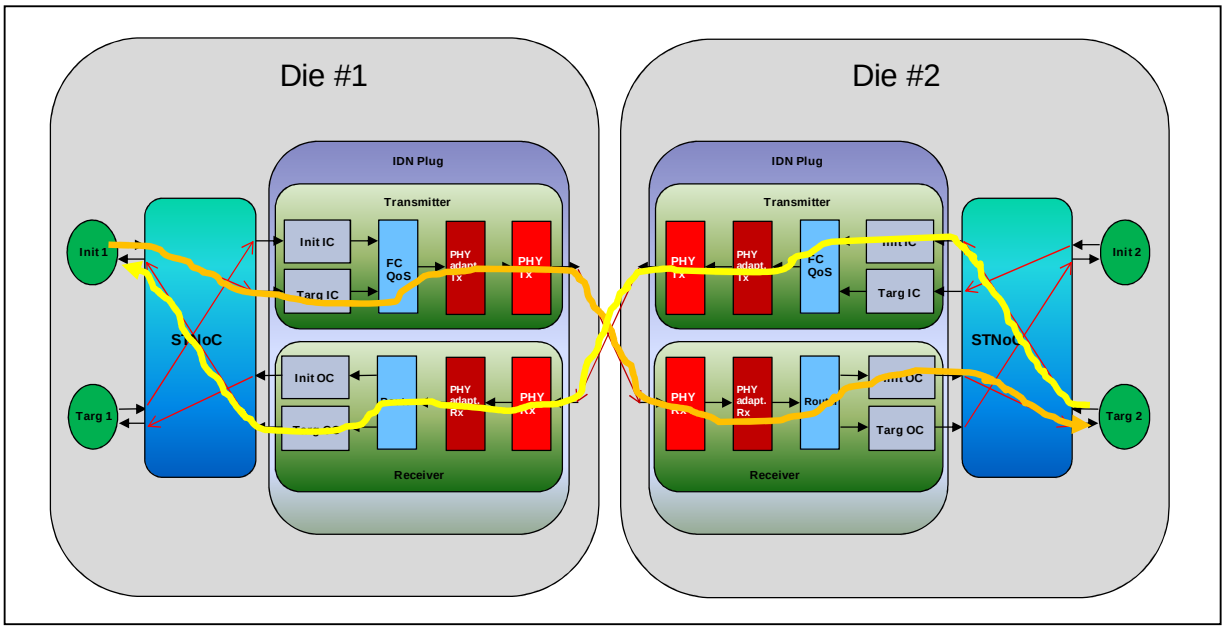

Figure 2-4 : Traffic streams flows between two dice

A detailed description of all the DDCM building-blocks can be found in deliverable D5.4 (Generic DDCM compatible with plasmonics-based PHY specification document).

4. DDCM PHY adapter

This section describes the DDCM PHY adapter able to interact with a plasmonics-based PHY.

The DDCM PHY adapter is responsible for adapting the System on Chip (SoC) traffic in such a way to be transferred between the two chips of the system across the physical channel.

Transmitter

The PHY adapter transmitter is responsible for transforming digital data into a format used to modulate the output of the plasmonic LASERs in order to transmit the data across the physical channel (plasmonic waveguide).
Figure 4-1 shows the microarchitecture of the DDCM PHY adapter transmitter, highlighting the digital blocks and the analog ones.

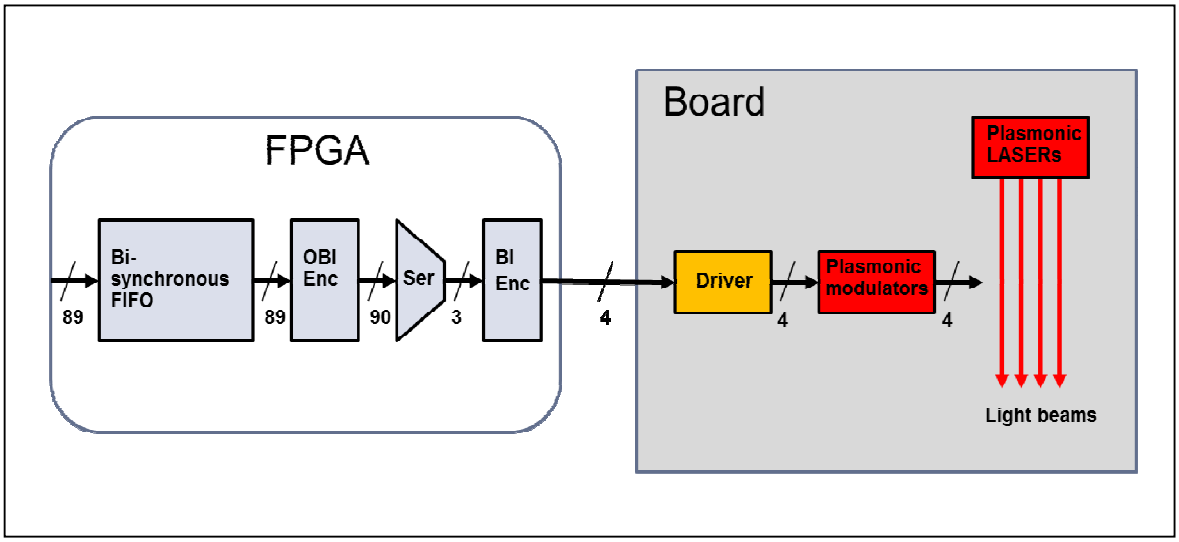

Figure 4-1: DDCM PHY adapter transmitter microarchitecture

The DDCM PHY adapter transmitter is composed of the following building-blocks:

- a **bi-synchronous FIFO**, playing the twofold role of retiming stage and storage element;
- a data encoder for the minimization of the number of '1' to be transmitted within a data word, in order to keep turned on the minimum number of plasmonic emitters (**Optical Bus Inverter Encoder**);
- a **serializer** to transmit the N-bits data as chunks of M-bits, exploiting the M plasmonic emitters; in the system used for the demonstrator, the input and the output of the serializer are 90 and 4 bits wide respectively.
- a **data encoder** for the minimization of the Hamming distance between two back-to-back data words, in order to minimize the switching activity of plasmonic emitters (**Bus Inverter Encoder**);
- a set of M **modulator drivers**, each generating the proper control signals for plasmonic LASER modulators;

Receiver

The PHY adapter receiver is responsible for the transformation of the plasmonic information got from the physical channel (plasmonic waveguide) into a format suitable to be used by the digital parts of the SoC.
Figure 4-2 shows the microarchitecture of the DDCM PHY adapter receiver, always highlighting the digital blocks and the analog ones.

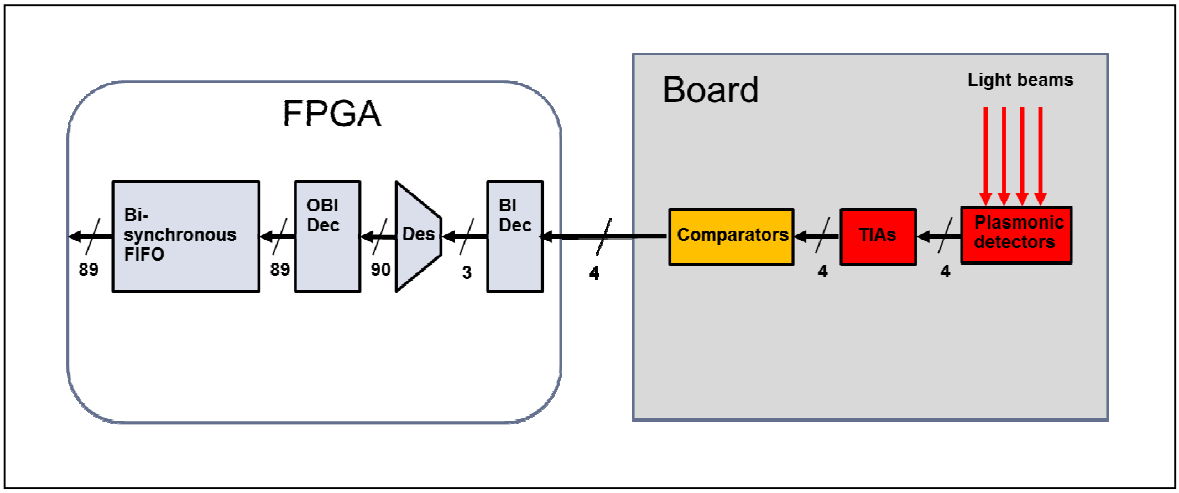

Figure 4-2: DDCM PHY adapter receiver microarchitecture

The DDCM PHY adapter receiver is composed of the following building-blocks:

- a set of M **Trans-Impedance Amplifiers** (TIAs) responsible for translating the output currents generated by the plasmonic photodetectors into voltage levels;
- a set of M voltage **comparators** responsible for associating the proper logic value (‘0‘ or ‘1‘) to the output of the TIAs;
- a **data decoder** for performing the inverse transformation applied to data words by the Bus Inverter Encoder in PHY adapter transmitter (**Bus Inverter Decoder**);
- a **deserializer** to merge the chunks of M-bits, coming from the M plasmonic photodetectors into a N-bits;
- a **data decoder** for performing the inverse transformation applied to data words by the Optical Bus Inverter Encoder in PHY adapter transmitter (**Optical Bus Inverter Decoder**);
- a **bi-synchronous FIFO**, playing the twofold role of retiming stage and storage element.

A detailed description of the DDCM PHY adapter able to manage a plasmonics-based PHY can be found in milestone MS5 (Digital domain to plasmonic domain interface specification and VHDL modelling).