Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Identification of possible contributions to the industrial partners for commercialization

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List of Partners concerned

Partner number	Partner name	Partner short name	Country	Date enter project	Date exit project
1	Karlsruher Institut für Technologie	KIT	Germany	M1	M36
2	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMEC	Belgium	M1	M36
3	TECHNISCHE UNIVERSITEIT EINDHOVEN	TU/e	Netherlands	M1	M36
4	RESEARCH AND EDUCATION LABORATORY IN INFORMATION TECHNOLOGIES	AIT	Greece	M1	M36
5	UNIVERSITAT DE VALENCIA	UVEG	Spain	M1	M36
6	STMICROELECTRONICS SRL	ST	Italy	M1	M36
7	UNIVERSITEIT GENT	UGent	Belgium	M1	M36

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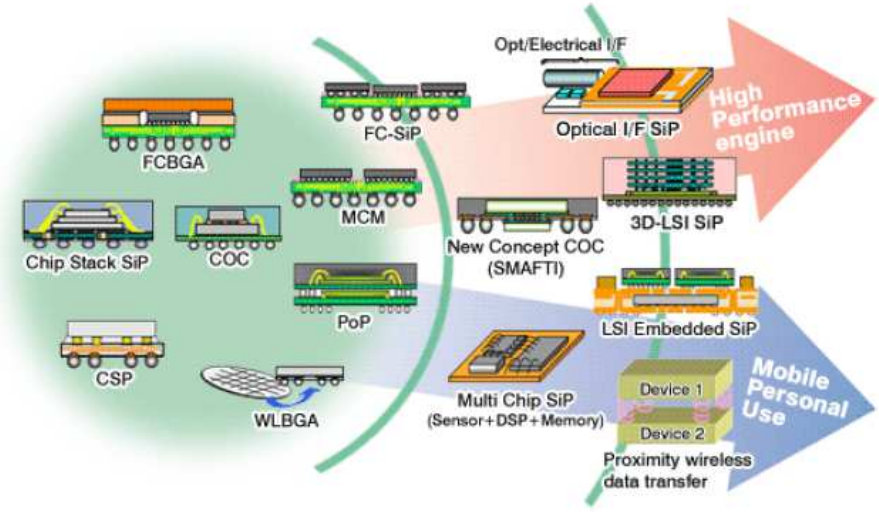
Executive Summary

Over the years, SiP (System-in-Package) technologies have gained huge popularity because of the many advantages they offer (1) and likely continue to grow in the future, following the market demand in portable applications, such as mobile phones or laptop computers, where the size and the power consumption represent the two major factors for a successful implementation (2). This document starts with a brief introduction to the SiP market trends, than it analyzes the approach of many Microelectronics Companies to SiP technology, their proposed solutions and future potential applications; finally it describes requirements and challenges required by new potential products in which SiP can be applied, from which the benefits offered by plasmonics appear relevant.



Advanced Packaging Technology Roadmap by NEC (3)

Change Records

Version	Date	Changes	Author
0.1 (draft)	2013-07-08	First version	Valentina Cernuto
1 (submission)	2013-07-31	Final version	Valentina Cernuto, Alberto Scandurra

Contents

1. Introduction

The market demand for increased performance, smaller size, lower power and lower cost cannot be met with conventional packaging and interconnect technologies. There are limitations in interconnect density, thermal management, bandwidth and signal integrity that cannot be addressed with conventional technology (4). System in Package Technology is perhaps the most important technology to overcome these limitations and, for this reason, the Microelectronics Industries have invested in SiP.

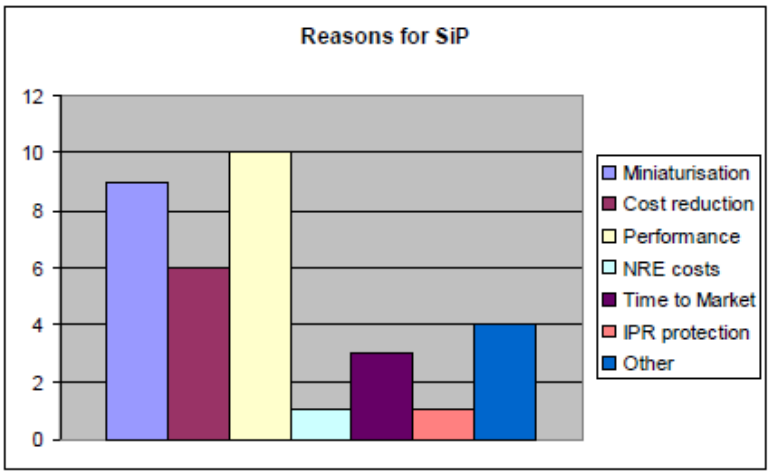


Figure 1-1: Reasons for SiP (5)

The first stacked packages utilized in market applications contained only memory and logic devices (6). Now SiP's family offers many solutions for different application and has rapidly penetrated most major market segments: consumer electronics, mobile, automotive, computing, networking, communications, medical electronics, etc.

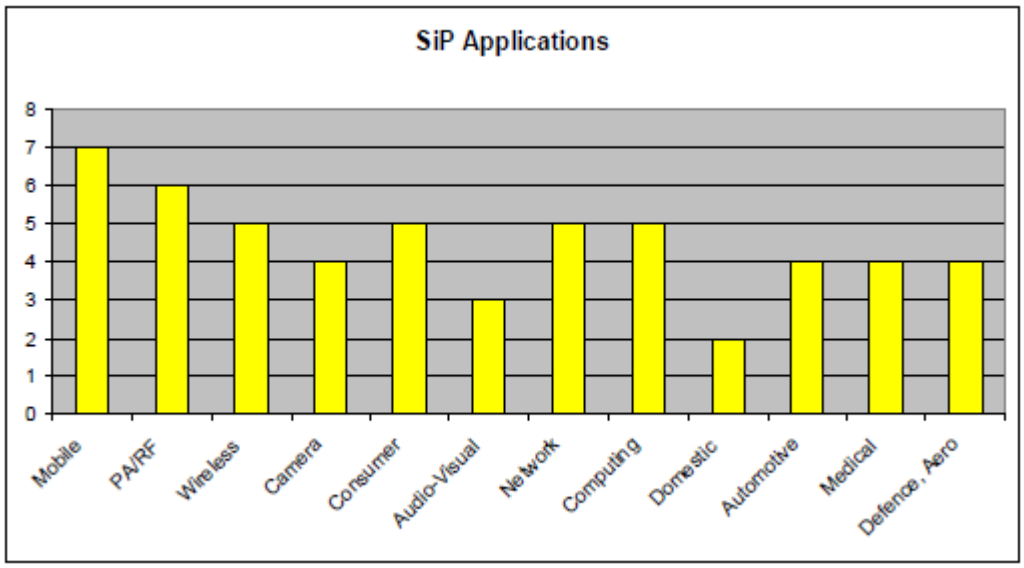


Figure 1-2: SiP Applications (5)

General requirements for SiP

The general requirements for SiP are many and depending on application but, typically, are small and specialized form factor, high functionality density, high frequency operation, thermal dissipation, large memory capacity, high reliability, low package cost, low development cost, fast time-to-market, wireless connectivity (GPS, Bluetooth, cellular, etc.) (4).

2. SiP Applications Review

In the following section are reported several SiP applications and the associated SiP technologies made by some Microelectronic Companies.

SiP is a product in which two or more chips conform a system utilizing the package's interconnect structure (7). It saves lead time, space, and BOM cost in the application. By including critical components into the SiP package and moving routing to the SiP, the system complexity, size and component placements can be reduced (7).

The fast growth of SiP technologies and the increased competitiveness of design solutions have created an economic opportunity and market imperative for many Semiconductor Industries. When one thinks about the types of products that use SiPs, the usual impression is that they are found mainly in small devices such as mobile phones, digital still cameras (DSCs), and digital video cameras (DVCs). Indeed, besides the well-known advantages of smaller size, slimmer profile, and lighter weight, SiP ICs offer other important benefits, including lower EMI noise, high-speed bus design, cost savings, faster development times, and security features. For this reason today SiP solutions are increasingly being adopted in comparatively larger devices that are not subject to particularly strong constraints on the space available for components (see Figure 2-1). Especially, there has been a rapid growth in customers using in SiPs in high-volume products such as freestanding digital TVs, printers, and optical disk drives (8).

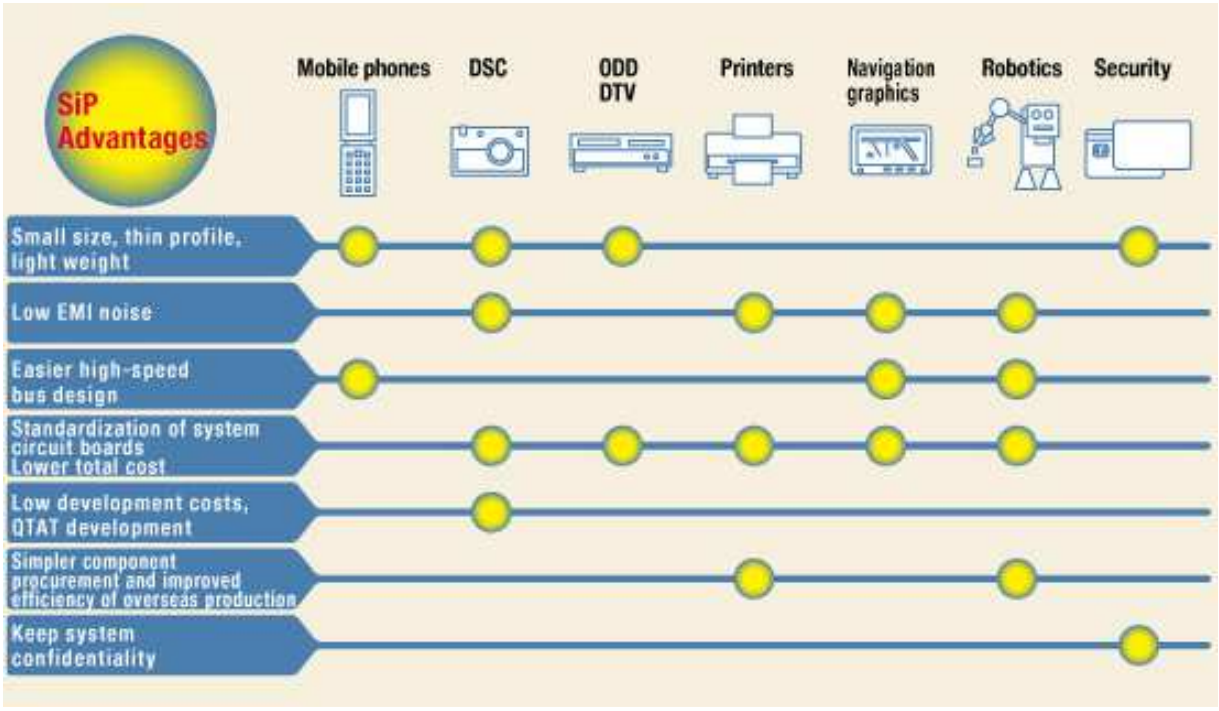


Figure 2-1: Uses and advantages of SiP Technology (9)

Renesas Electronics

Renesas SiP has various structures and those characteristics are shown below (7).

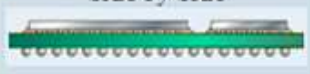
Structure	Advantage	Flexibility of Memory vender	High Density	Heat Dissipation	Cost
Chip Stack 	Small and High-density Circuits	☆	☆☆☆	☆☆	☆☆
Side by Side 	Good heat dissipation	☆	☆	☆☆☆	☆
QFP 	Low Cost	☆	☆	☆☆	☆☆☆
PoP (Package on Package) 	High Flexibility of Memory vender	☆☆☆	☆☆	☆☆	☆

Figure 2-2: Structures and Characteristics of SiP (7)

SiP design process used by Renesas is shown in following figure.

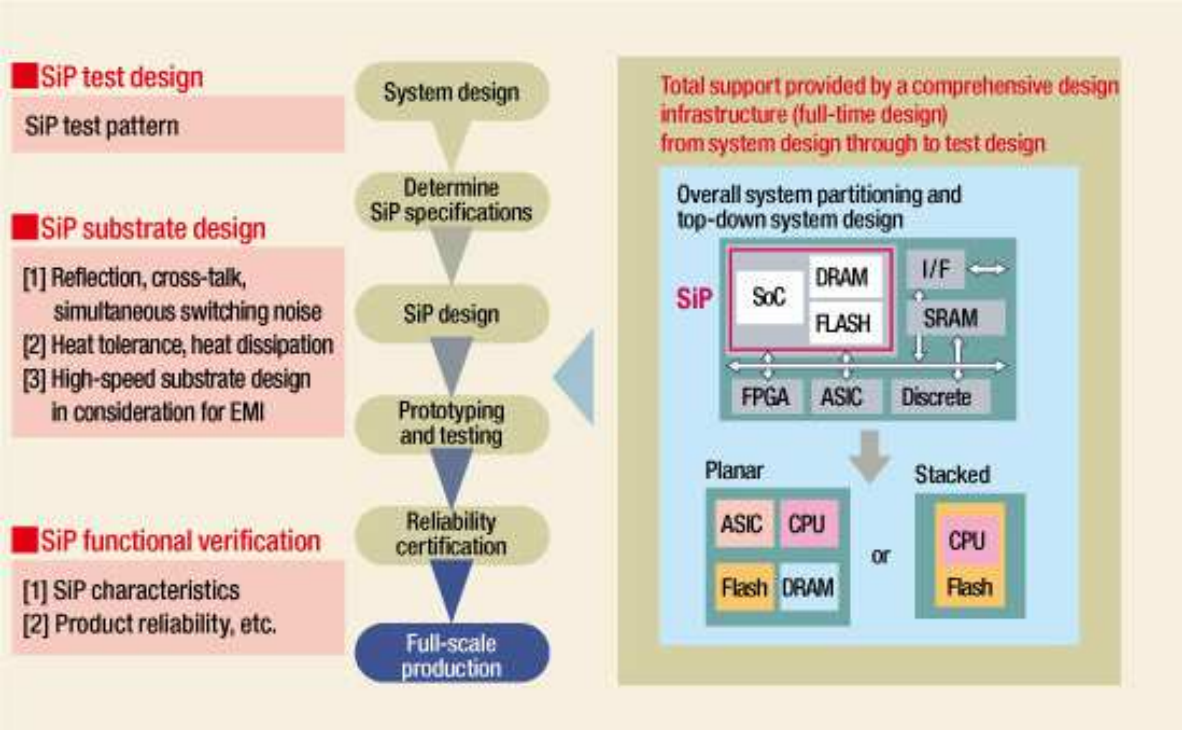


Figure 2-3: SiP design process (7)

SiP products can be broadly divided into two categories: stacked SiPs, in which the chips are placed on top of each other (3D IC) and planar SiPs, devices in which the chips are laid out horizontally. Stacked SiPs are particularly effective for achieving miniaturization and increasing component density. By contrast, planar SiPs help meet design requirements such as lower noise, ease of high-speed bus design, high reliability, high heat dissipation, and security. In terms of the external package dimensions, most SiPs smaller than 15 mm square are stacked types, whereas those 16 mm square or larger are mostly planar types (see following figure) (9).

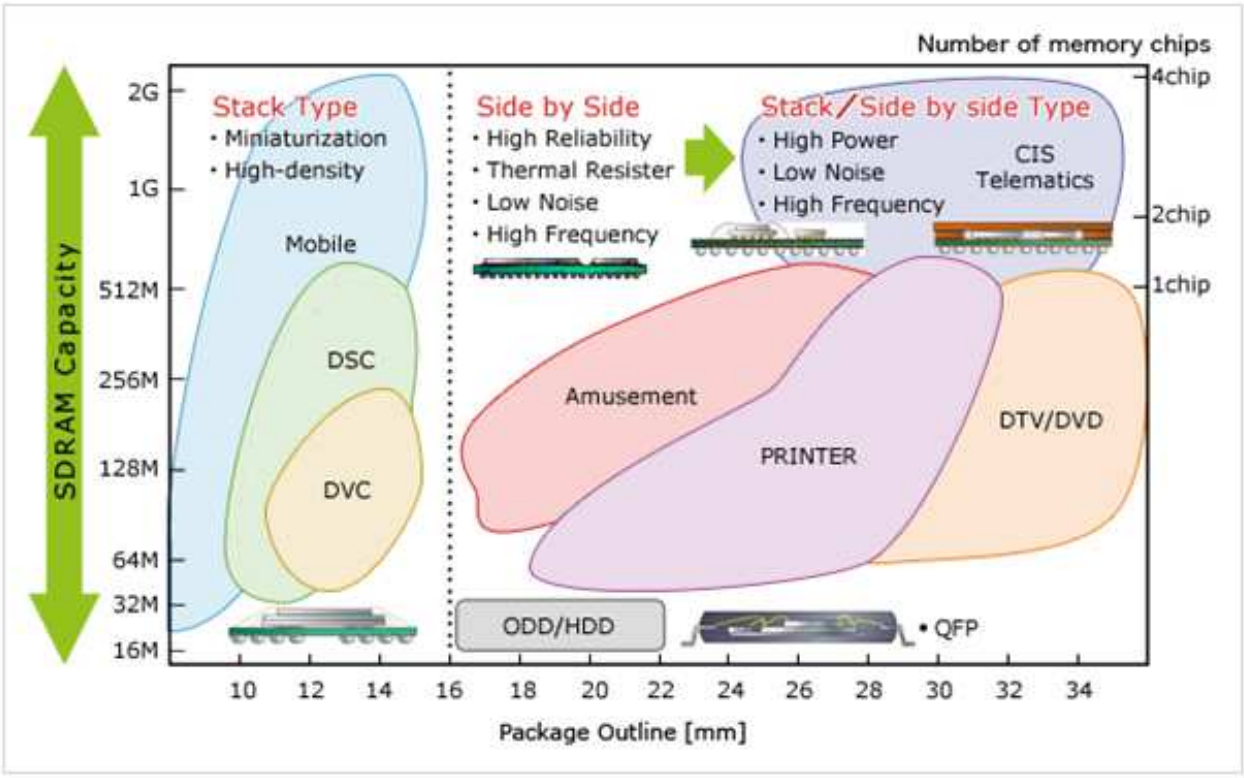


Figure 2-4: The relationship between SiP external dimension, structure and DRAM capacity (9)

In terms of the combination of chips installed in the latest Renesas SiP solutions, an increasing proportion of them contain a SoC and DRAM. A main reason for this is that the memory capacities of DRAM chips are getting larger and manufacturing costs make it difficult to integrate DRAM into the SoC device itself. Another reason is that the speed of the DRAM I/O bus is rising due to faster SoC and microcomputer processing speeds, making it more difficult to properly design the wiring connections between the SoC and DRAM (9).
Renesas has established a comprehensive design infrastructure for new SiP products and has implemented flexible SoC design using the DFS (Design for SiP) methodology. "Design for SiP" means designing SoCs using a methodology that takes account of SiP requirements (see Figure 2-5) (9).

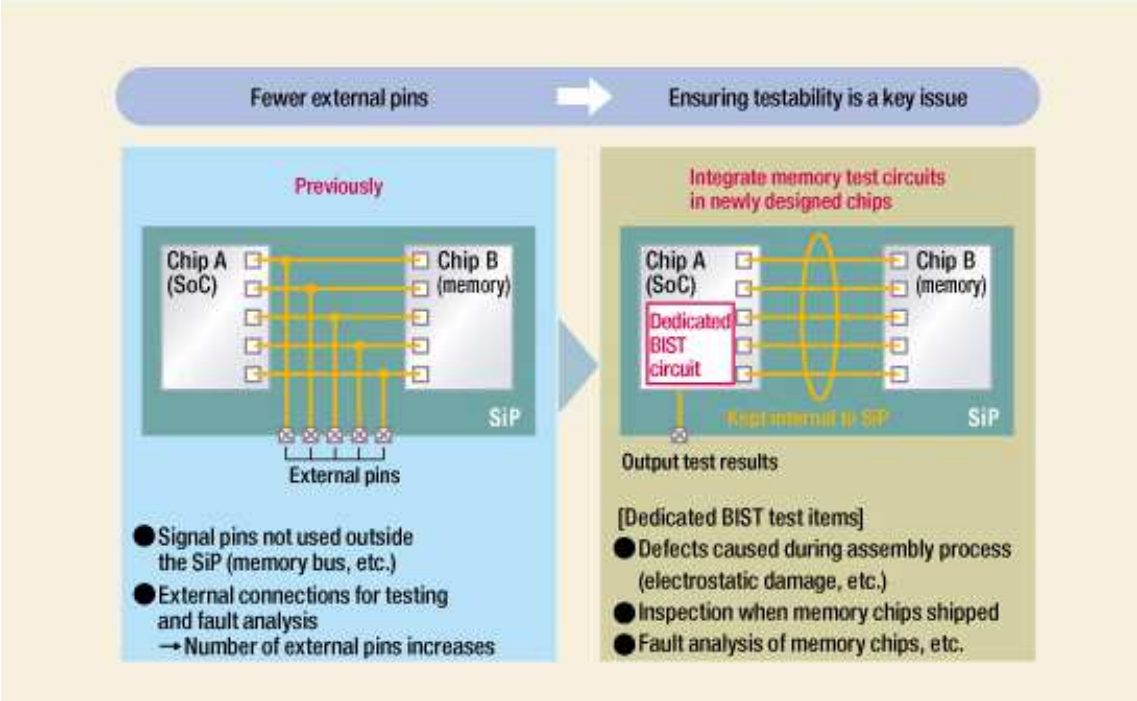


Figure 2-5: Example of how SoC design takes into account SiP requirements (9)

On some SiPs that combine an SoC with memory, Renesas integrates the memory BIST (Built-in Self Test) circuit into the SoC device (see Figure 3-5), an approach that reduces pin count of the SiP because pins are no longer needed for the memory test function (9).
The Renesas advanced package technologies, employed by SiP to connect multiple chips in a package, are shown in the following figure (7).

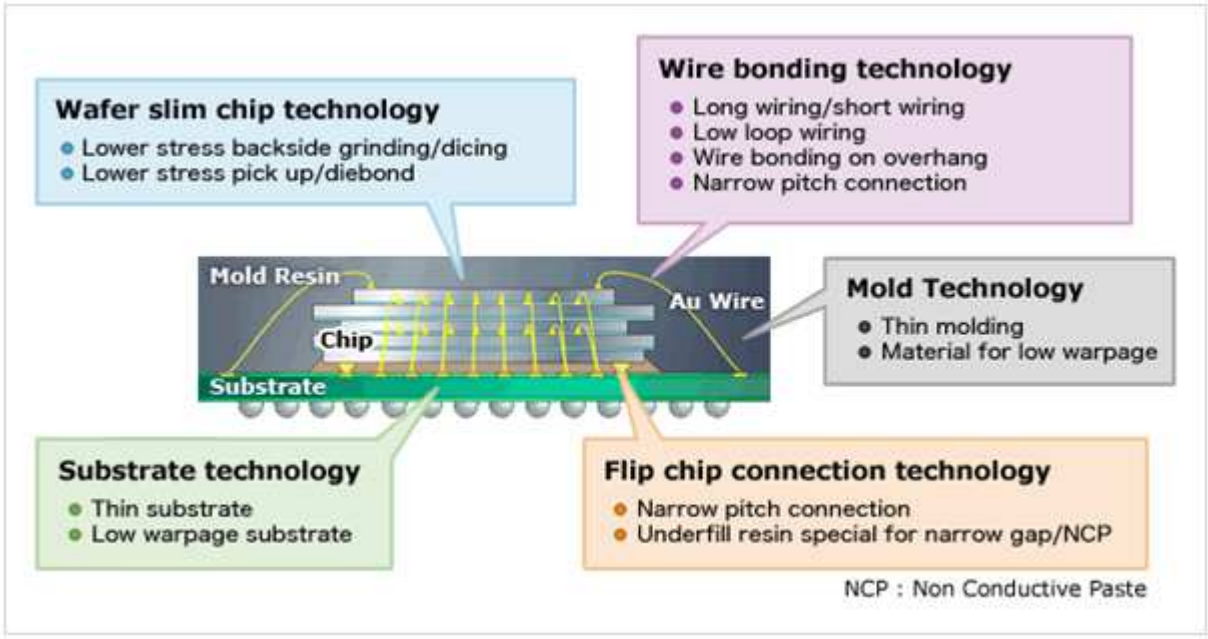


Figure 2-6: Key Technology Supporting SiP (7)

For stacked SiPs, their portfolio of individual technologies includes low-mold technology with a mounting height of 1.5 mm or less and methods for thinly machining the wafer underside with low stress (thicknesses of 70 μm are used in full-scale production). They also apply technology for wire bonding with a pitch of only 30 μm, flip-chip connection technology that can produce more than 700 pins with a pitch of 40 μm or less, and technology for producing ultra-thin 0.2 mm SiP substrates (see Figure 2-7) (9).

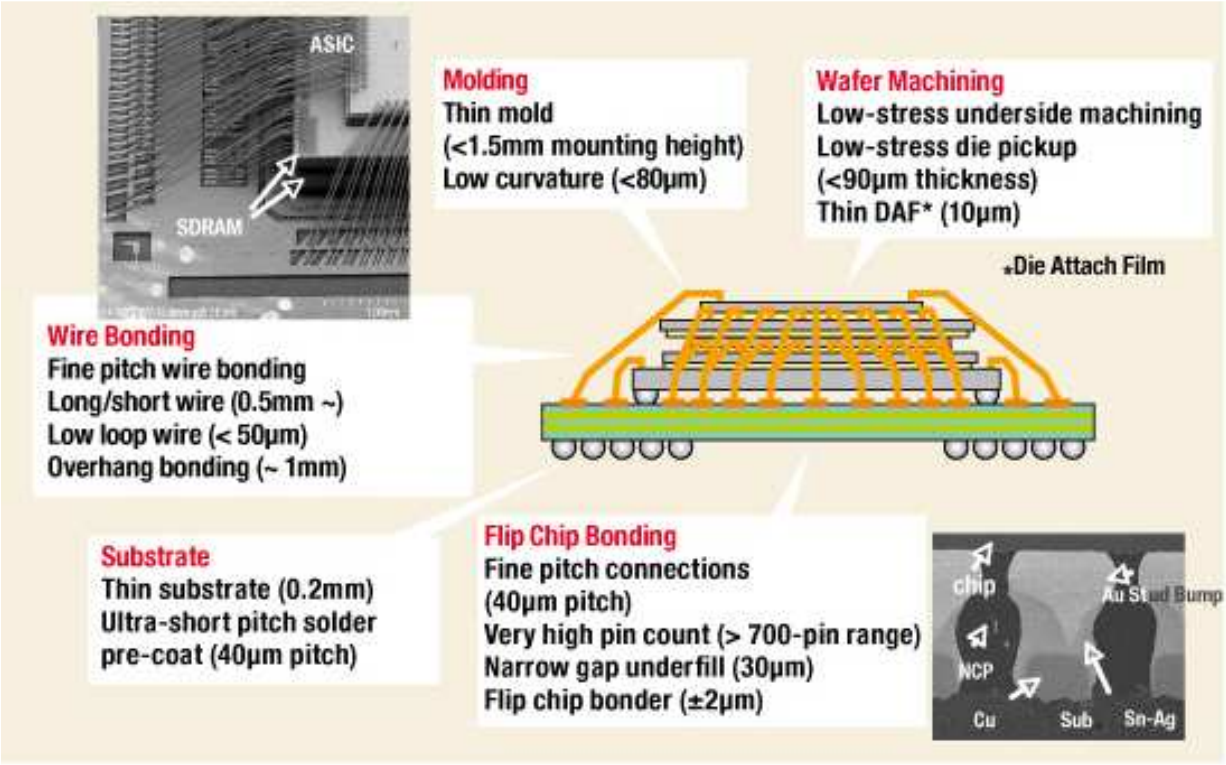


Figure 2-7: Technologies used in stacked SiP (9)

A development that provides the ultimate in miniaturization and thinness is the through-silicon electrode technique that Renesas is developing jointly with Hitachi.
This technology involves making holes in the silicon wafer and forming electrodes between the upper and lower surfaces. The through-silicon electrode technology can reduce the height of SiP packages by more than half. For this reason it appears to have great potential for use in future SiP devices (9).

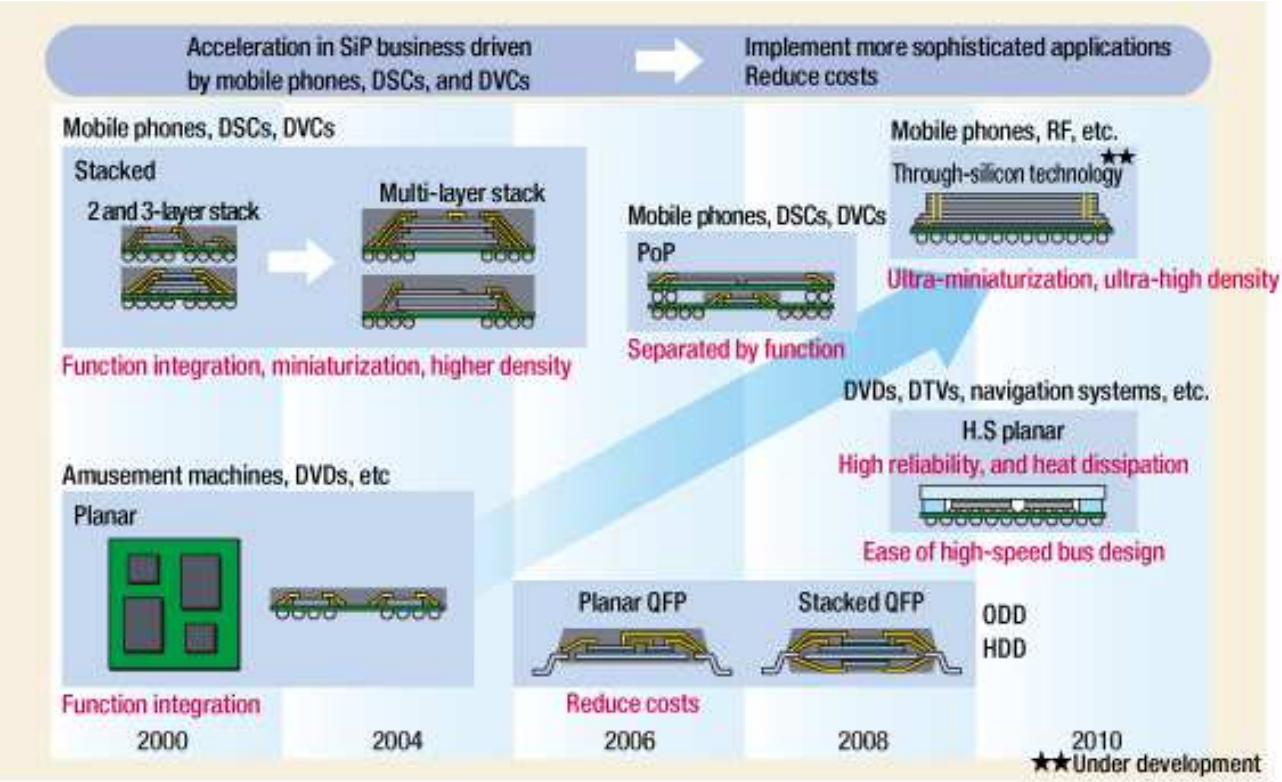


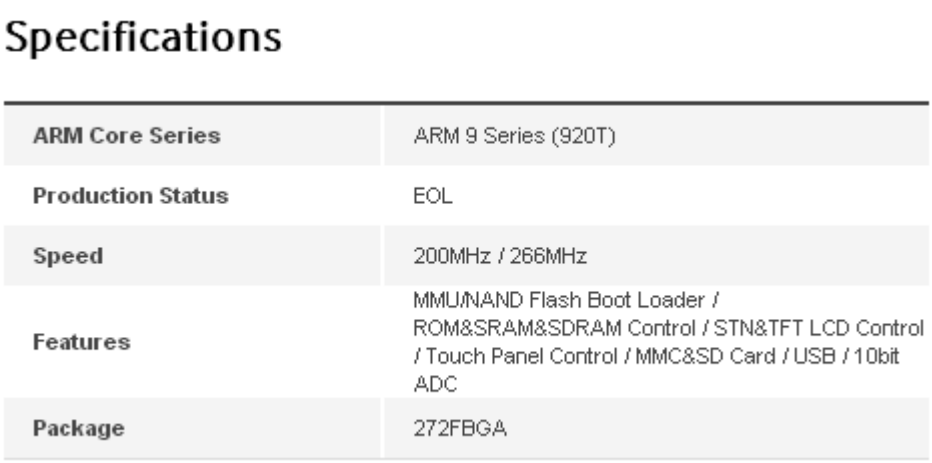
Figure 2-8: SiP structure and Roadmap (9)

Samsung Electronics

In 2003 Samsung announced the industry's first System-in-Package with an ARM-based processor, Nand flash and SDRAM for next-generation mobile phone and handheld applications. The new SiP solution integrates advanced logic and memory technology into a single package, reducing component count and shrinking form factors for handheld devices. This gives PDA (Personal Digital Assistant) and Smartphone designers the flexibility to create a new range of cell phone designs and form factors that also support advanced features such as multimedia. The most important requirements for a PDA and a Smartphone are:

- higher performance;
- longer battery life;
- increasing memory density.

The SiP's small form factor, 17x17mm square in size and 1.4 mm high, integrates Samsung's S3C2410 ARM-based application processor, 256Mb of NAND flash memory and 256Mb of SDRAM memory. The S3C2410 has been the world's first SoC to have a NAND flash boot loader (see its specifications in Figure 2-9).



Specifications

ARM Core Series	ARM 9 Series (920T)
Production Status	EOL
Speed	200MHz / 266MHz
Features	MMU/NAND Flash Boot Loader / ROM&SRAM&SDRAM Control / STN&TFT LCD Control / Touch Panel Control / MMC&SD Card / USB / 10bit ADC
Package	272FBGA

Figure 2-9: S3C2410

The S3C2410 features an ARM920T CPU core operating at 203 MHz. The chip supports major operating systems including Microsoft Windows CE, Palm OS, Symbian, and Linux. The S3C2410 SOC offers a set of tailored peripherals for Smartphone and other handheld devices. For example, the S3C2410 application processor includes USB host and device support to allow connectivity to a variety of other devices including PC's, printers, removable storage, and other handhelds. The processor also has SDIO support, which allows handhelds to be accessorized with upcoming SDIO protocol devices such as digital cameras, keyboards, etc (10).
In 2005 Samsung presented at the Samsung Mobile Solution Forum (Taipei, Taiwan) the first System-in-Package containing a 300MHz mobile CPU, a 1Gb NAND flash memory and 256Mb mobile DRAM, a 260K color display driver IC (DDI) for active matrix OLEDs (organic light emitting diodes), a qVGA resolution one-chip DDI and a 2.5-inch qVGA TFT LCD for MP3 players. The high density mobile DRAM, high-performance logic-CPU design accommodate the increasingly large data processing and storage needs of portable game consoles, handsets, camcorders and personal data assistants (PDAs). By combining memory and system LSI technology, Samsung is coupling proven components within advanced package technology to improve mobile system integration, reduce power consumption and minimize size limitations. SiPs also reduce interference between devices, adding significantly to system reliability (11).
The Korean electronics giant recently updated its Packaging Roadmap, including recent advancements in the commercialization of high performance 3D SiP with TSV (Through silicon via) interconnects (see Figure 2-11). On the roadmap presented in figure 3-12, Samsung clearly shows a strong interest for introducing 3D into logic + memory and logic + logic stacking applications. These two last configurations are now the main driving forces to implement 3D into next generation PoP (Package on Package) and SiP applications such as mobile processors, CPU and high performance ASICs (Application Specific Integrated Circuit). The main drivers for 3D here are cost and performance (12).

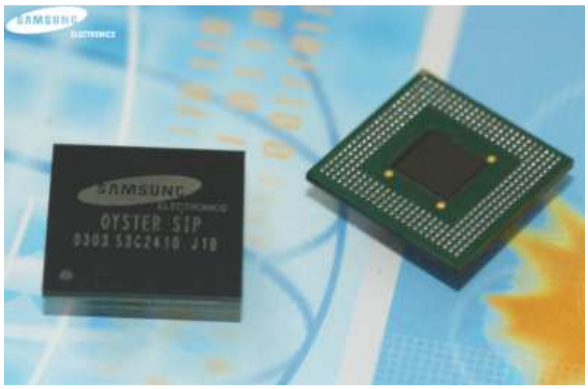


Figure 2-10: Samsung SiP

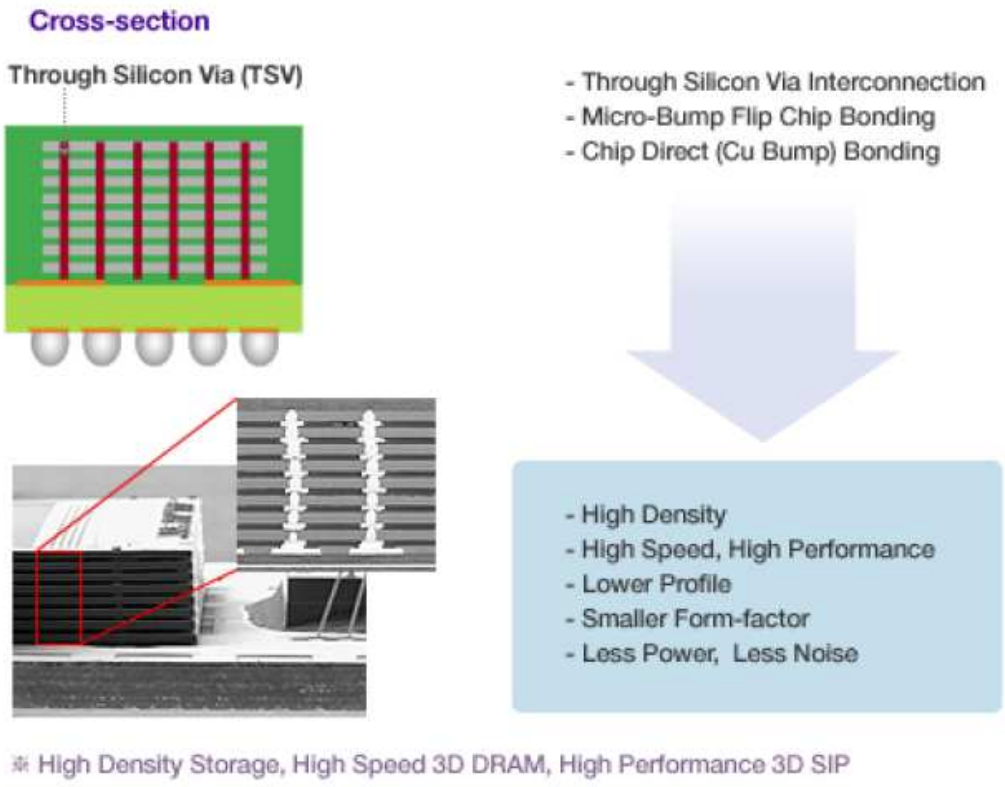


Figure 2-11: Through Silicon Via (TSV) (13)

The advanced future showed in the new 3D TSV Packaging Roadmap is 3D Optoelectronic Integration (13).

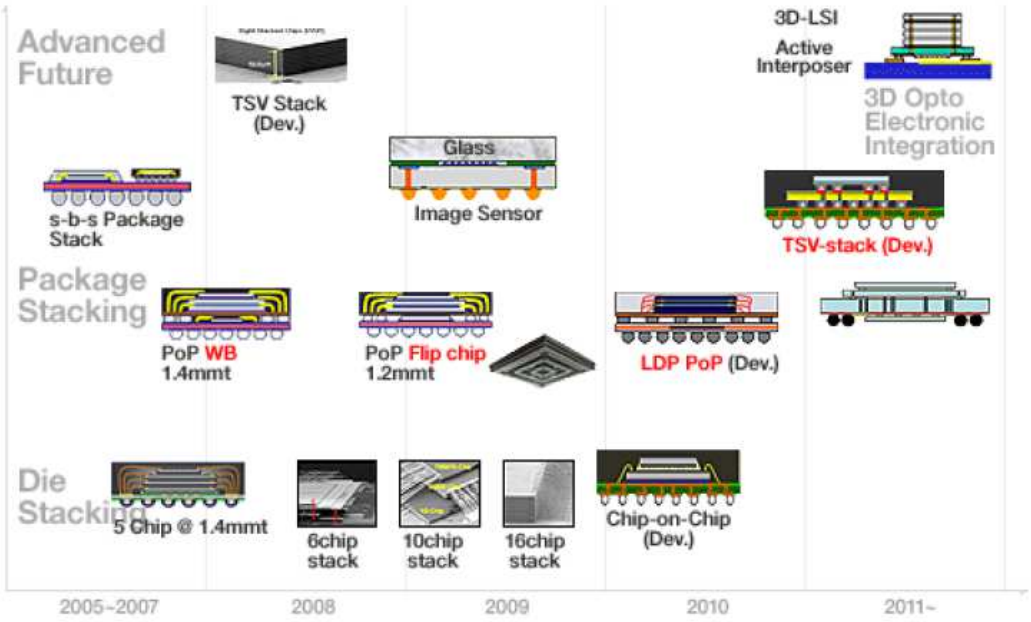


Figure 2-12: Samsung Roadmap (13)

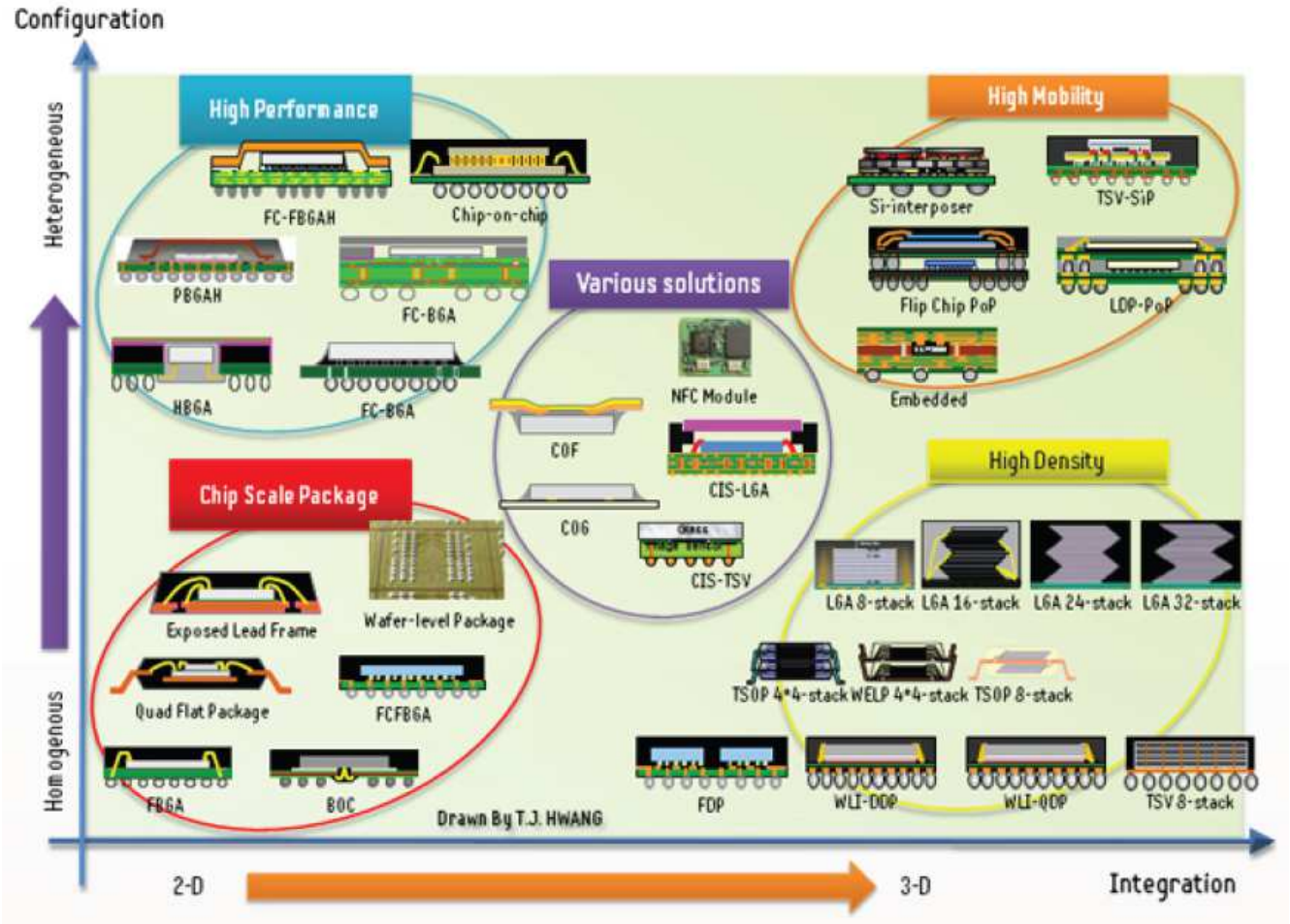


Figure 2-13: Samsung's Competitive edge in Packaging Technology (13)

Philips

Philips has also chosen SiP but believes in a careful combination of SiP and SoC technology because it is the best solution for mobile wireless devices (14).
In 2005 Philips launches on the market a SiP containing a digital TV receiver DVB-H-based for mobile phones. Low power operation is a key requirement for TV-on-mobile solutions. The SIP, together with the TV tuner and the demodulator, consumes less than 50 mW of power in DVB-H mode, consuming 300 mW in continuous mode. It currently comes in a small module package measuring 15x25x2 mm, shrinking next year to 9x9x2 mm (15).

Amkor Technology

System-in-Package approaches are being revisited by Amkor now that silicon interposers with copper pillar interconnects have demonstrated increased I/O capacity, speed, and bandwidth (reduced latency) and a reduction in power consumption (16). The silicon interposer and copper pillar bumps facilitate the integration of massive quantities of interconnect logic and on-chip resources within a single package, allowing the resulting SiP to deliver exceptionally high improvement in performance.
Fine-pitch copper pillar flip chip and complex package assembly will bridge the gap between today's SoC constraints and successful SiP execution (17).
Existing market uses for Amkor SiP include RF and wireless devices (such as power amplifiers, GPS modules, digital cellular, Bluetooth® solutions), Netbooks, digital baseband solutions for the wireless markets and controllers for hard drives in the storage market.
Amkor has RF design engineers on staff to assist customers in designing RF SiPs, including creating circuit elements (e.g., baluns and filters) in the substrate which may eliminate discrete components. Amkor is able to meet all design, material and manufacturing requirements for RF SiPs, including such items as wire length control and substrate materials (LTCC, laminate and others). Amkor has successfully used its RF design and packaging capability to integrate shields and antennas directly into the SiP (18).

Toshiba

The evolution of mobile electronic devices such as cell phones, digital cameras, digital camcorders and portable audio players is driving the demand for SiP solutions (19).
Some examples of SiP applications are shown in the following figures.

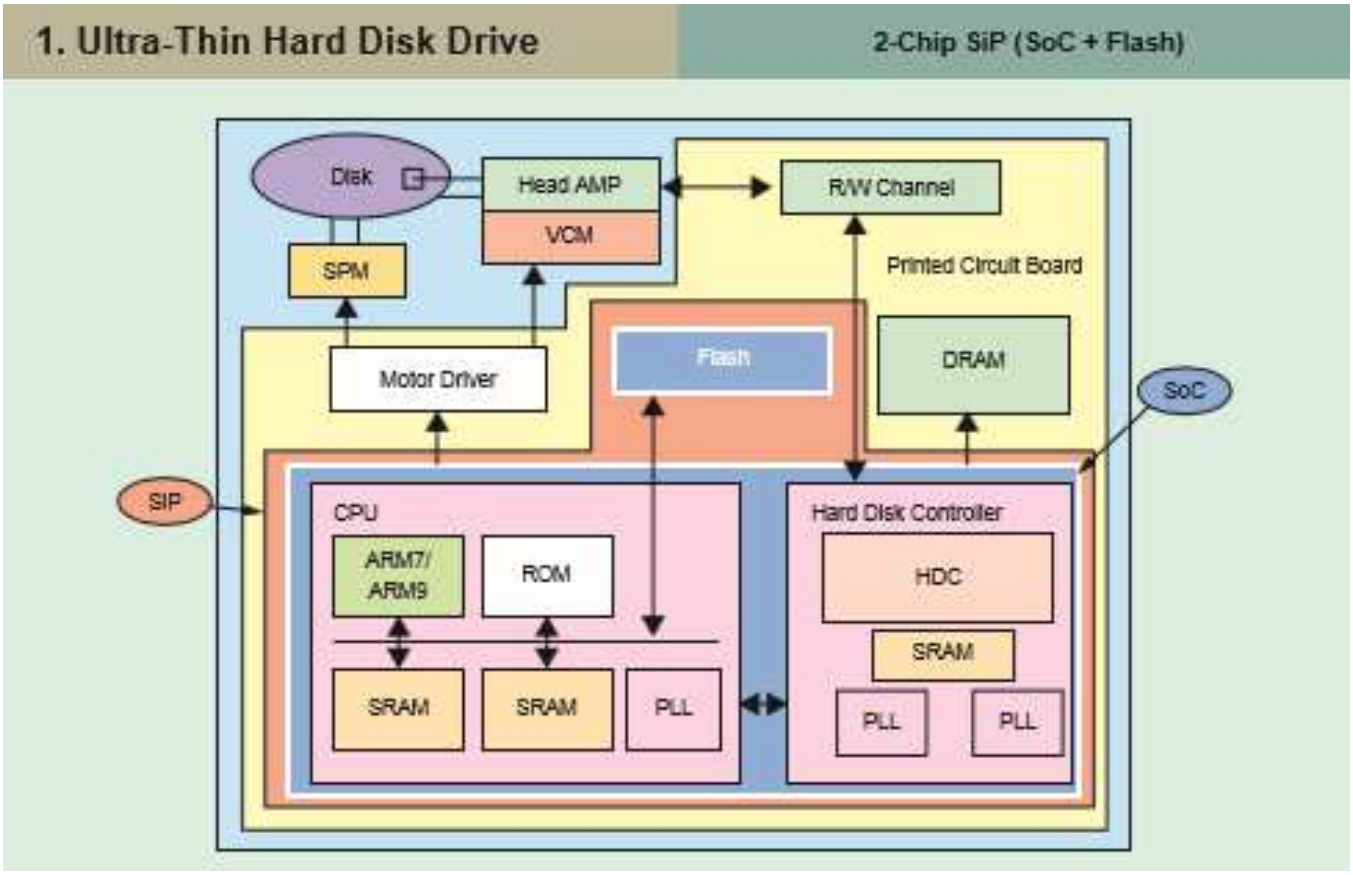


Figure 2-14: Example SiP Application (19)

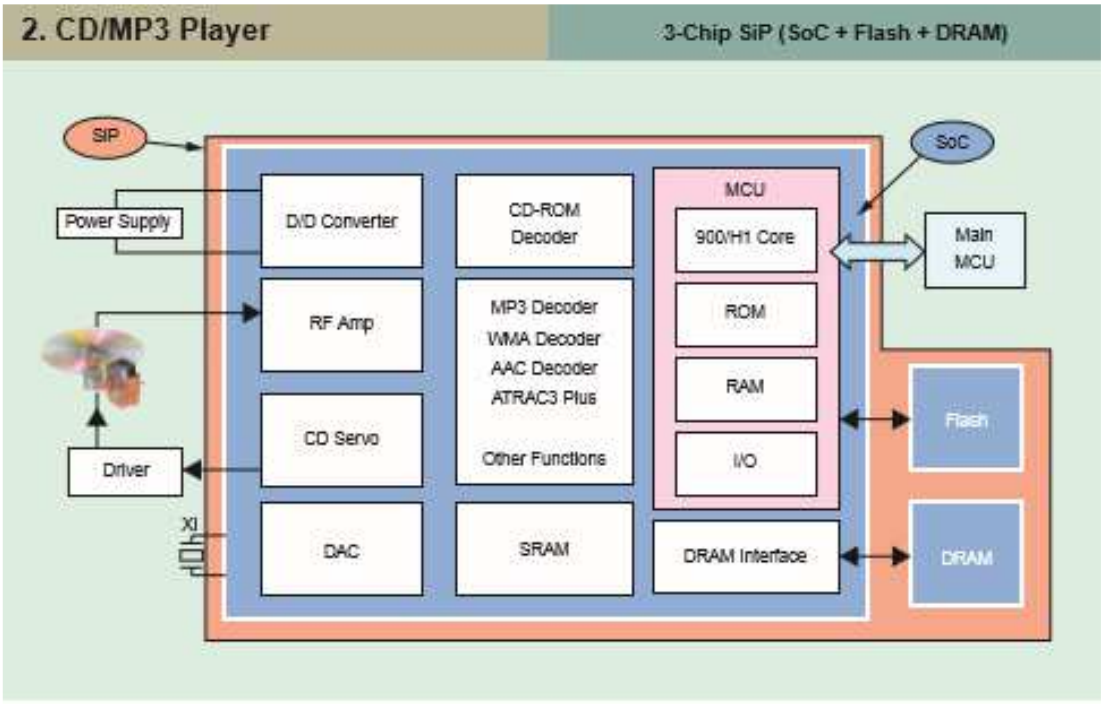


Figure 2-15: Example SiP Application (19)

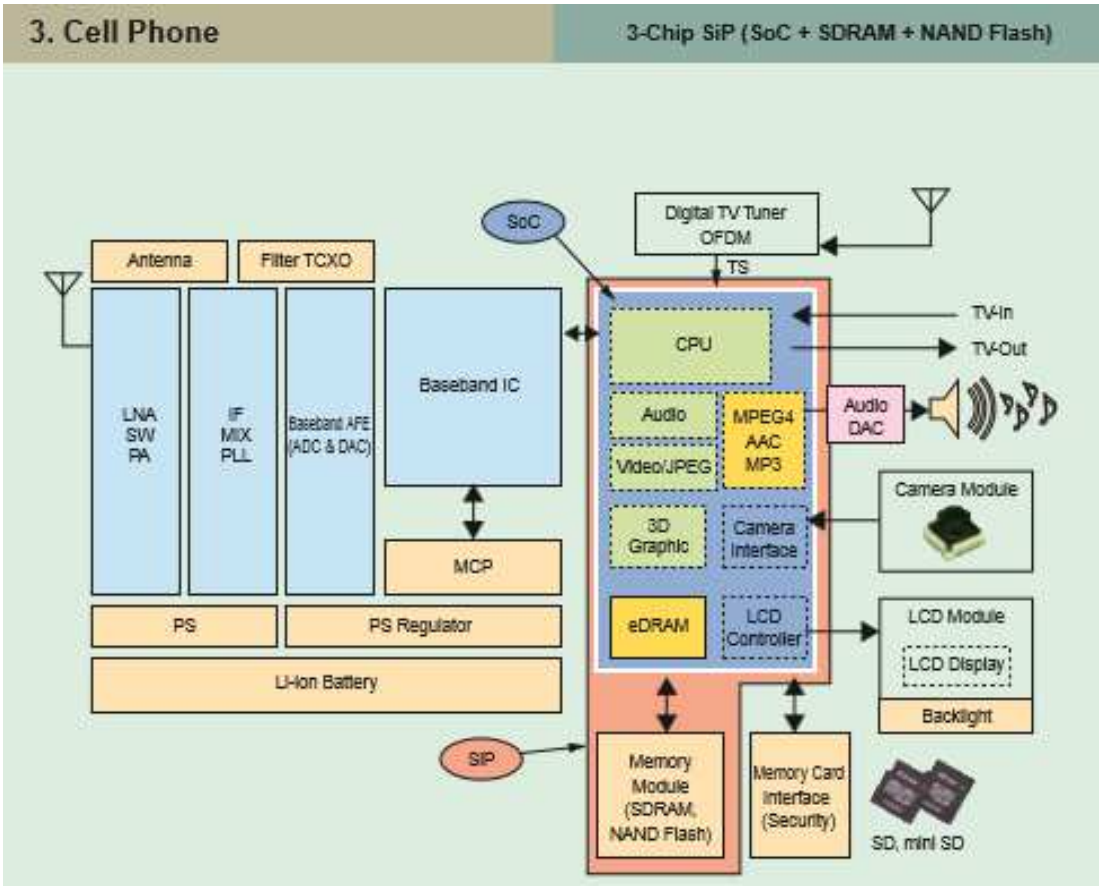


Figure 2-16: Example SiP Application (19)

CPUs	TX99, TX49, TX39, TX19, TLCS-900/H1, TLCS-900/L1, ARM9, MeP
Memory (Incl. Third-Party Products)	NOR Flash, NAND Flash, FCRAM, SRAM/DDR-SRAM
User Logic	0.18µm, 0.13µm, 90nm
Digital IP	USB 2.0, IEEE 1394, 10/100BASE Ethernet MAC, Audio Codec (MP3, etc.)
Analog IP	DC-DC Converters, A-D Converters

Figure 2-17: IP Core Offerings (19)

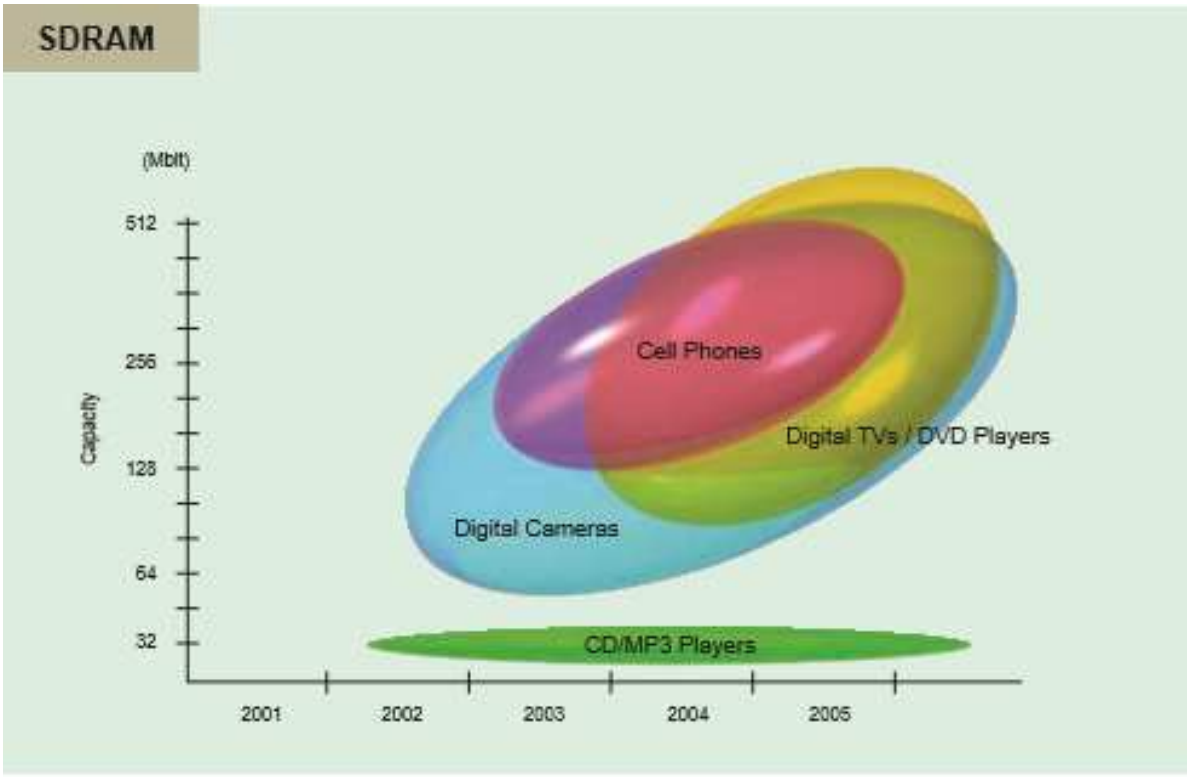


Figure 2-18: SiP Memory Trends (19)

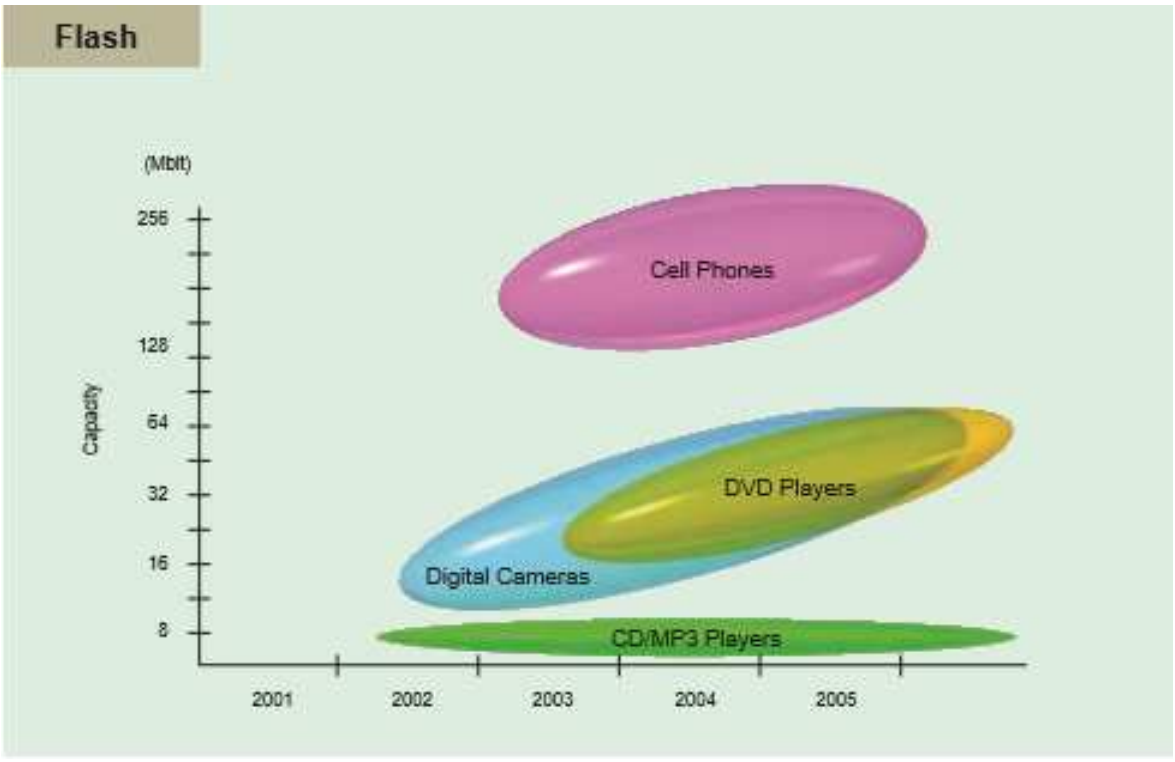


Figure 2-19: SiP Memory Trends (19)

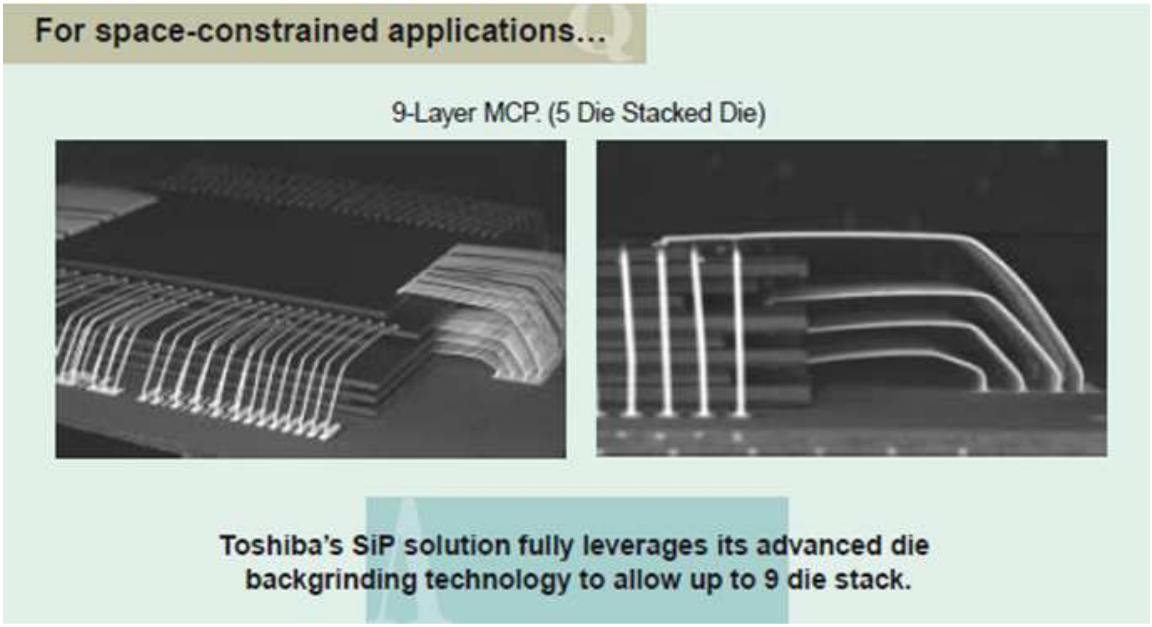


Figure 2-20: High-Density Packaging Technology (19)

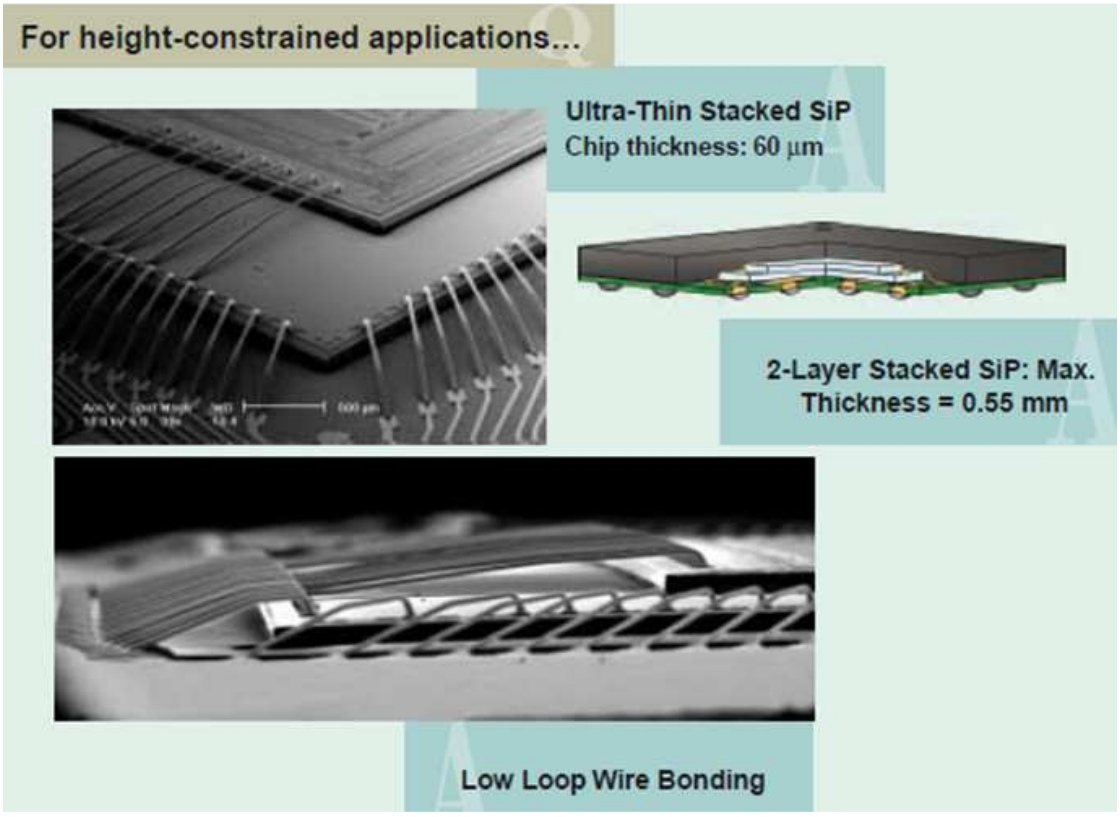


Figure 2-21: High-Density Packaging Technology (19)

Atmel Corporation

With the rapid LIN[2] market growth, the requirements for ever-increasing system efficiency, higher integration and lower costs have increased as well. Similarly, the number of control switches for various applications has also increased. Applications where the switches are located very remote from the control electronics and wires integrated within the wiring harness do require high-voltage switches. The Atmel ATA6642 SiP has been developed to fulfill these increasingly demanding market requirements. The new ATA6642 LIN SiP is designed for complete LIN-bus node applications, in particular for LIN switch applications. Integrating almost the complete LIN node, the device consists of two ICs within one package. The first chip is the ATA6641 LIN SBC, encompassing a LIN transceiver, a 5V regulator (up to 80mA load current), a window watchdog, an 8-channel high-voltage switch interface with high-voltage current sources and a 16-bit SPI for configuration and diagnostic purposes. The second chip is the Atmel AVR® ATtiny167 automotive 8-bit microcontroller with advanced RISC architecture and 16KB Flash memory. With its industry-leading design, the ATA6642 offers designers great flexibility, so that the SiP can be used in various applications such as port/contact monitoring, switches (towards GND or VBAT), LED/ relay/ power transistor control or switches connected through the wiring harness (20).

Intel Corporation

In November 2010 Intel Corp. unveiled the first six members of its line of system-in-package products announced in September. The products include an Atom and Altera FPGA die. The FPGA blocks allow engineers to customize the devices for whatever interfaces or unique features their system requires.

The high–end chip uses a 1.3GHz Atom with a 400MHz graphics block consuming 3.6W and costing $106. The low-end device runs at 600MHz with a 320MHz graphics block, consumes 2.7W and costs $61.

The Altera FPGAs inside the 37.5 mm package use more than 60,000 logic elements and can support six high-speed transceivers using more than 350 I/O pins. The transceivers can run at up to 3.125Gbps or support LVDS links with SerDes at 840Mbps.

The FPGAs can be programmed with the Altera Quartus II Subscription Edition tools. They include PCIe logic, DSP multipliers and some internal memory.

Formerly codenamed Stellarton, the Intel Atom processors E665CT, E645CT, E665C, and E645C are scheduled to be available within 60 days (21).

CeraMicro Technology Corporation

As a SiP design house and solution provider, they focus on their Passive & Discrete components Database development for different purpose on RF application. They also focus on speed in design process, their manufacturing Ceramic substrates and RF Module products. CeraMicro's SiP solutions on LTCC (low temperature co-fired ceramic) was the pioneer in Taiwan to embraces Taiwan's IC and with their specific Passive components to complete the functional module, with their strategic Manufacturing Partners, CeraMicro can provide customer the total solution of SiP from concept to complete products in mass production. They provide from total RF module solution to only LTCC ceramic substrate design:

Design for consumer RF module:

- WiFi 802.11 a/b/g ~n module;
- Bluetooth Module;

[2] LIN: low-cost local interconnect networking is a serial protocol used for in-car communications.

- Front End Module…. etc.

Radar Defense subsystem:

- 2-18GHz Frequency Synthesizers.

Module Substrate:

- LED application;
- WiFi 802.11 a/b/g~ n substrate;
- Bluetooth module substrate;
- Front End Module substrate.etc.

As with System on Chip (SoC), CeraMicro SiP technology is an ideal solution in markets that demand smaller size with increased functionality. SiP is the modular design approach offering unprecedented flexibility in product development (22).

SiP RF Module

Item	Product Name	Product Description	Remark
1	RFM-M-01	WiFi 802.11 a/b/g Module - WLAN IEEE 802.11 a/b/g	Module Size: 8.2x8.4x1.3 mm
2	RFM-M-02	"WiFi+BT" Combo Module - WLAN IEEE 802.11 b/g - Bluetooth 2.1+EDR	Module Size: 9.5x9.5x1.3 mm 
3	RFM-M-03	"WiFi+BT+GPS" Combo Module - WLAN IEEE 802.11 b/g - Bluetooth 2.1+EDR - GPS	Module Size: 15x15x1.3 mm 
4	RFM0502	WiFi a/b/g 1T1R Front-End Module - PA, Switch, diode, Multiple dies - BSF, BPF, Coupler, Doplexer Embedded	Flexible-Applied for WiFi+BT; Integrated for Handset Platform

Figure 2-22: SiP RF Module

Sharp

Sharp Corporation is the first manufacturing that has developed a technology with 0.5 mm – ball pitch for 3D SiP. This technological innovation has enabled to put DSP, Flash Memory and SDRAM in one stack (14x14x1.7 mm). The module base containing the DSP in only 0.25 mm – substrate is put in the space product by the ball pitch. The second module, which contains 32Mbit Flash Memory and one or two 256Mbit SDRAM, is put on base module. Consequently, the assembly surface becomes smaller. Using this technology, Sharp has made and brought into market two LSI systems whose features are:

- Model: LR38683/LR38682
- Voltage Operation: 3,0÷3,6V
- Configuration:1x32Mbit Flash Memory, 2x256Mbit SDRAM/1x32Mbit Flash Memory, 1x256Mbit SDRAM
- Pixel Range DPS: 3,0÷10 millions
- Time Memory Access: 10 ns (Flash Memory)
- SDRAM Frequency: 100MHz
- Dimensions:14x14x1,7mm (std)

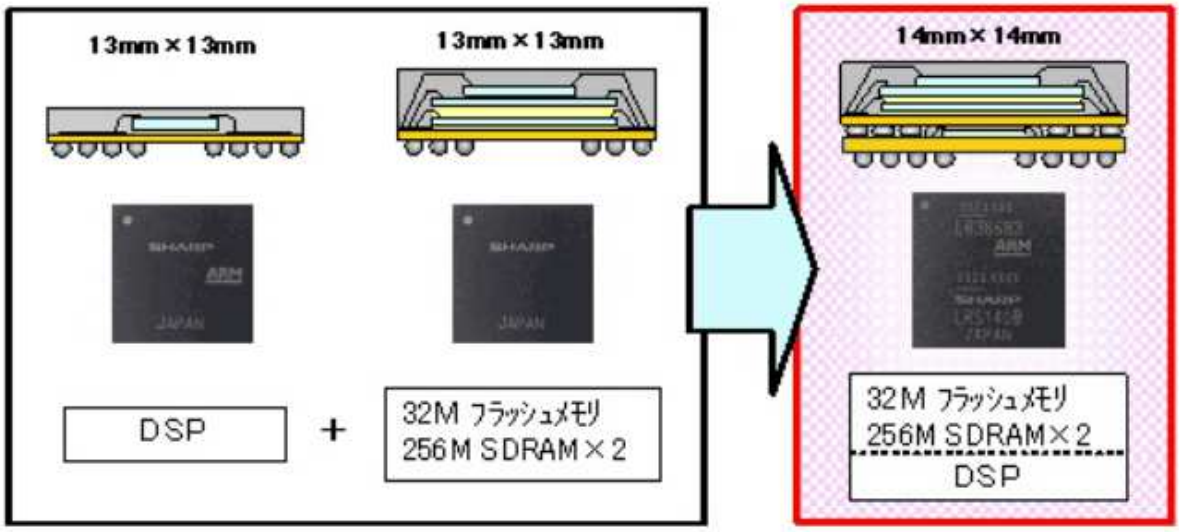


Figure 2-23: New technology 3D SiP developed by Sharp

(Start Volume Production: June 2005) (23)

These systems have been designed by Sharp specifically for digital camera but the 3D SiP technology is ideal for handheld devices as well as mobile phones (23).

STMicroelectronics

STMicroelectronics has given a strong impetus to the approach SiP for the next generation of MEMS (Micro Electro-Mechanical Systems): in particular, according to the company's plans by the end of 2013 will be available wireless MEMS components while in 2014 should be available MEMS gas sensors for environmental applications. ST has faced many challenges in the digital field in recent years and the results obtained in MEMS line have been very remarkable to the point of pushing the company to the top spot for sales proceeds (approximately $ 900 million in 2011) and for supremacy technology of MEMS. The system-in-package approach adopted by ST is based on different production processes for the sub-systems, and this is one of the reasons for the success. ST MEMS include a mechanical die, a die for conditioning and calibration of the analog signal and a die, as digital interface, that can contain a microcontroller. The next step will be to include an RF transceiver for wireless communications. To implement the RF function, ST uses two dice: one for the MEMS and second for the analog amplification, calibration and conditioning of signal. A third silicon component acts as a cover for the MEMS. The radio features of the next MEMS are designed for applications below 1 GHz with a data rate programmable from 1 to 500 kbps. Initially, the new wireless MEMS devices will be addressed to fitness and wellness applications. Another application field will be represented by the systems for monitoring tire pressure (24).

Freescale Semiconductor

Freescale Semiconductor uses SiP Technology to develop 18-20 mm - devices for 3G mobile phones.

The MC1321x family is Freescale Semiconductor’s ZigBee platform technology with a low power, frequency band 2.4GHz RF transceiver and an 8-bit MCU Memory in a 71-pin LGA package. The MC1321x family also offers broad range of integrated peripherals and interfaces

including I2C, SCI, Timers/PWM, KBI, as well as an 8 channel 10-bit ADC. The combination of the radio and microcontrollers, as well as the incorporation of key peripherals and functions, in a small footprint package allows for a cost-effective solution (25).

Freescale Part No.	Channels	Package	Supply Voltage (V)	Frequency Band (GHz)	MCU Memory	Application	Communication Protocal
MC13211	16	LGA, 71-pin	2 to 3.4V	2.4GHz	16KB	2.4GHz ISM	SIMPLE MAC
MC13212	16	LGA, 71-pin	2 to 3.4V	2.4GHz	32KB	2.4GHz ISM, 802.15.4	IEEE 802.15.4
MC13213	16	LGA, 71-pin	2 to 3.4V	2.4GHz	60KB	2.4GHz ISM, ZIGBEE	IEEE 802.15.4 or BeeStack

Figure 2-24: MC1321x family (25)

STATSChipPAC

STATSChipPAC's System in Package is a substrate based package with one or more IC's, multiple passives and other surface mount components with plastic over molded encapsulation. The use of advanced assembly techniques, such as flip chip, die stacking or a combination of both, allows mixed technology IC's and other components to be combined in a cost effective and reliable package with minimal footprint and maximum functionality. In addition, this package can be built either as a Land Grid Array or Ball Grid Array to match the application or thermal/electrical design requirements (26).

Package Configurations: a variety of Wire bond, Flip Chip and Stacked Die configurations are in production and under development. In addition, many standard package configurations can be integrated to address customer specific solutions (26).

Features

• Body sizes up to 50 x 50mm
• Flexible ball and land grid arrays
• Lead-free and green materials set
• Multiple routing layers and dedicated ground/power planes available for improved electrical performance
• BT laminate materials, Si backplane
• JEDEC standard compliant

Specifications

Die Thickness 60 - 355µm (2.4 - 14mils)
Gold Wire 0.6 - 1.3mil diameter, 99.99% Au

Applications

• RF/Wireless: Power amplifiers, baseband, transceiver modules, Bluetooth, GPS, UWB, etc.
• Consumer: Digital cameras, handheld devices, memory cards, etc.
• Networking/Broadband: PHY devices, line drivers, etc.
• Graphics processors

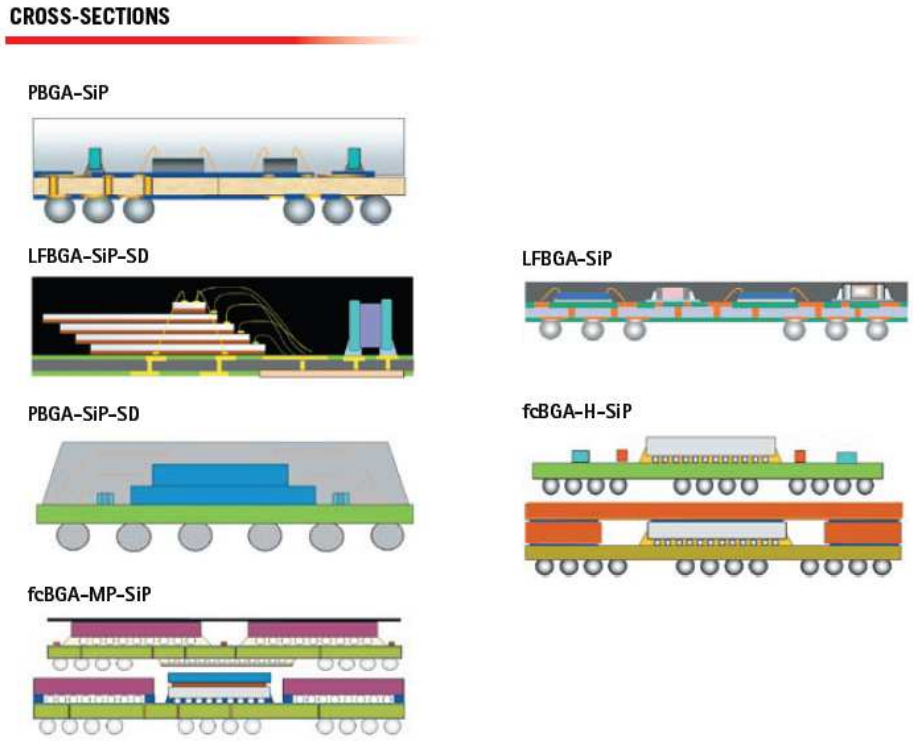


Figure 2-25: Cross-Section Different Configuration Packages (26)

IBM

3D Semiconductor & Packaging Technology for Systems

Three dimensional (3D) semiconductor and packaging technology using through-silicon-vias (TSVs) are used to stack thinned semiconductor chips and to integrate heterogeneous semiconductor technologies into micro-electronic modules.

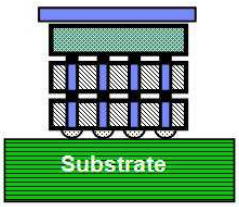


Figure 2-26

These microelectronic modules permit miniaturization which can be applied to portable microelectronics systems including: smart-phones, sensors and bio-medical solutions. The modules can also be applied to large computing systems such as servers and super-computers as well as many other applications.

Product applications can benefit from 3D technology to improve performance, increase bandwidth, improve power efficiency, and reduce costs. The 3D technology is developed at IBM's Thomas J. Watson Research Center and other IBM Research laboratories around the world. The IBM research teams drive 3D technology advancements including: materials, structures, processes and equipment to develop semiconductor wafer fabrication processes compatible with TSV's, wafer thinning and backside processing.

The research team also drives design and 3D integration technology advancements such as bond and assembly, test, module integration, power delivery and thermal / cooling solutions to support multiple generations of the technology for product applications.
The research team has been developing 3D technology for more than a decade and first products began shipping from IBM manufacturing in 2008 (27).

Research Data and Demonstration Examples:

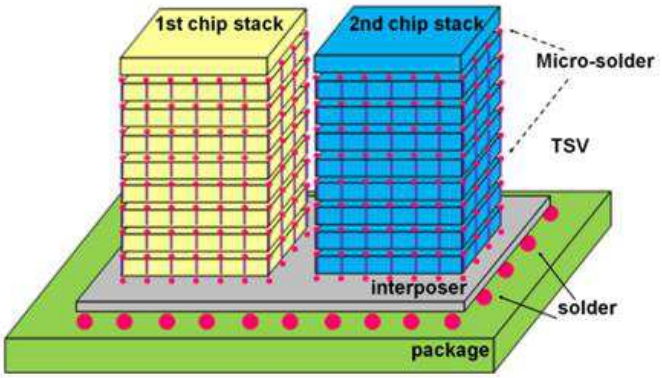


Figure 2-27: Design & Modeling as for electrical power distribution assessments in 3D chip stack (27)

Fujitsu

Fujitsu will provide the most suitable SiP to the customer's requirements with their extensive implementation technologies. Electronic products have been in growing demand, such as personal computers, mobile phones and PDAs, and its technology innovation has constantly come along. The IC technology is supporting customers to meet market demands today and in the future.
Packaging solutions enable to reduce size and space requirements as a key technology. The packages such as CSP (Chip Size Package or Chip Scale Package) and BGA (Ball Grid Array) have supported high-density wiring technology and widely used in the market. Miniaturization forced the use of new approaches in die packaging in order to achieve the smallest possible solutions. Leading the van of CSP, Fujitsu Semiconductor has launched the mass-production of SON packages which was impressed as the world's smallest level.
Fujitsu Semiconductor has a mass-production lineup of super compact packages such as FBGA (Fine Pitch BGA) and WL-CSP (Wafer Level CSP) and beyond. The high pin count packages, PBGA (Plastic BGA) and TEBGA (Thermal Enhanced BGA) have been mass-produced in order to fulfill the size and weight limitations, for example portable equipment.

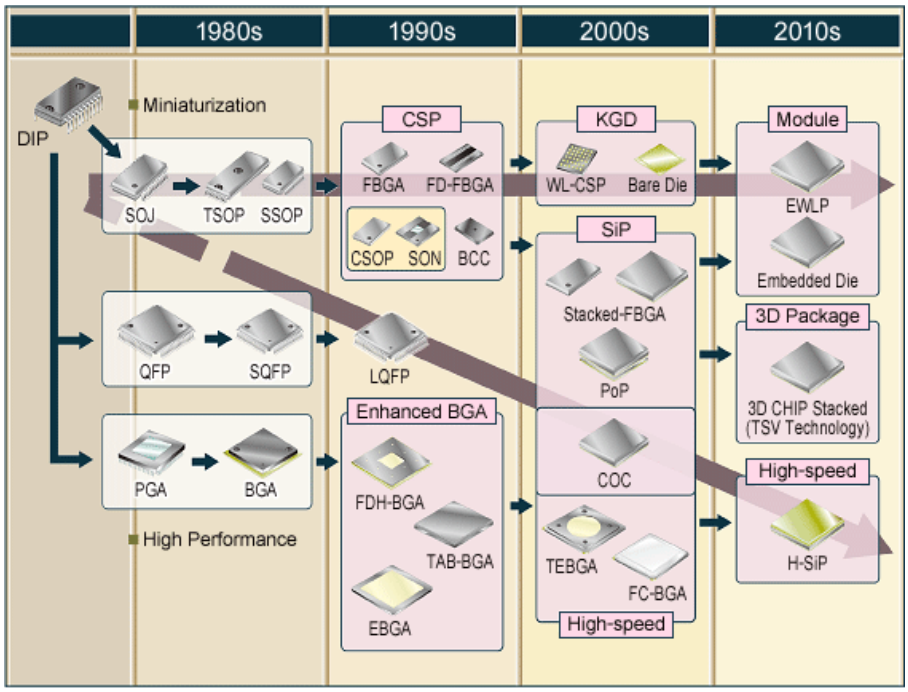


Figure 2-28 (28)

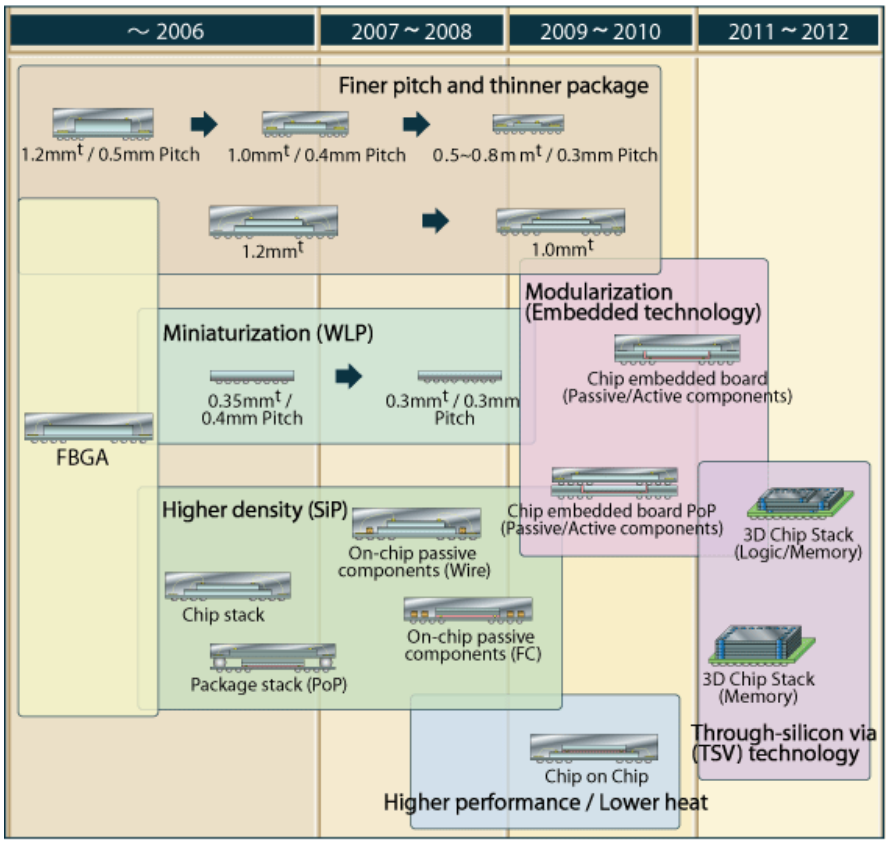


Figure 2-29: FBGA (Fine Pitch Ball Grid Array) Roadmap (28)

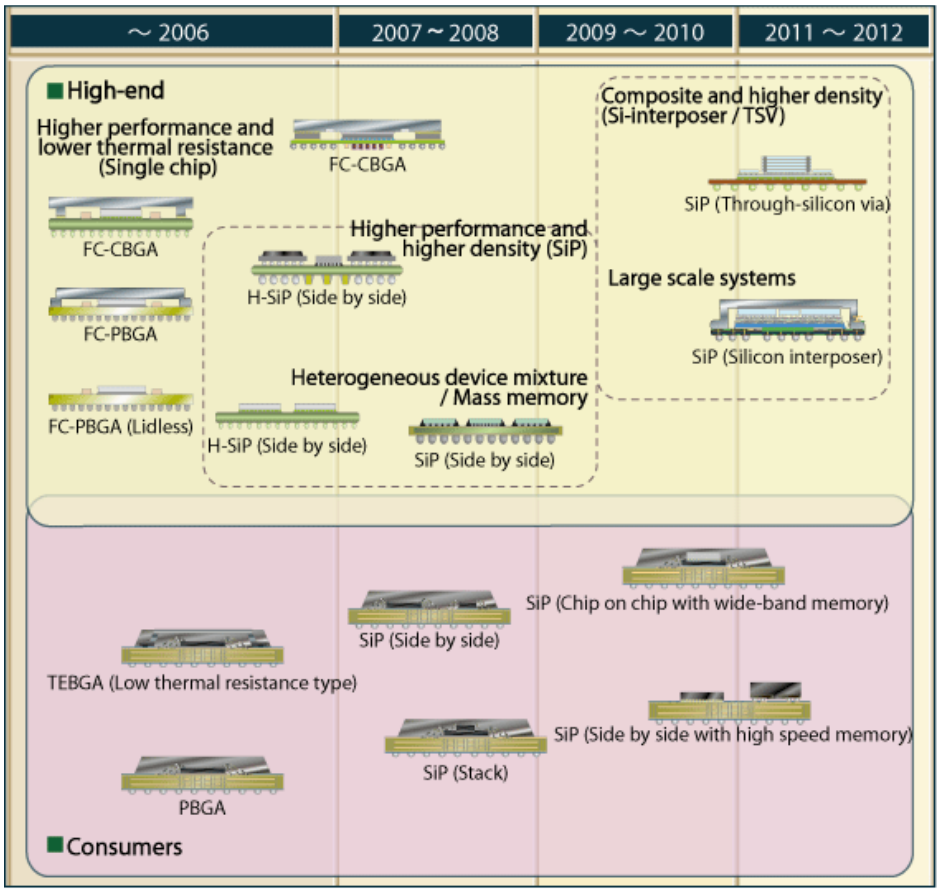


Figure 2-30: Multi-pin BGA Package roadmap (28)

3. Requirements for performance

Electrical Performance Issues with SiP

Interaction between different dice

Electrically, signal integrity and power integrity of the entire package must be maintained through careful design of the package (4).

- ***Signal integrity of a SiP***

1. In terms of signal integrity of a SiP, *cross-talk* is a very important issue due to the increase in signal count and reduction in physical spacing between traces connecting different dice at the package level. Giga-Hertz signal transmission presents a challenge in a SiP, especially, in a thin film environment, where dielectric thickness may be restricted due to materials and process limitations. The increased signal density causes a decreased signal line widths and then transmission loss. Signal integrity may be further degraded due to *reflections at impedance discontinuities* such as I/O pads to substrate interconnects or embedded vias.
   In a mixed signal SiP, where digital and analog circuits may reside closely in a single module, sensitive analog traces must be properly isolated from fast digital traces. Circuits

generate noise that can couple to other circuits on the same die or within the same SiP, also known as *substrate coupling or substrate noise*.
High performance circuits, such as PLL or high-speed digital links, are more sensitive to electromagnetic interference noise and electromagnetic interference remains a major challenge for SiP integration.
Solution: innovative designs are in need to enhance or replace the conventional approaches like physical separation and barriers (4).

2. Furthermore, *timing skew* and *impedance matching* may also be an issue due to the increases in signal count and operating frequency. Groups of traces need to meet timing constraints, which may require physical layout iteration due to signal crowding and trace impedance requirements. Additionally, traces may be physically long causing unacceptable parasitic capacitance, resistance, and inductance values. The higher wiring density required for SiP forces narrower traces and therefore increases interconnection inductance. For example, the bond wire of a die that is stacked on 3 other dice will have higher inductance values than the bond wires of the 3rd die in the stack, which will in turn have higher inductance values than the bottom flip-chip as in the case of a hybrid stacked SiP. This will significantly affect signals waveform as they undergo transients (4).

- ***Power Integrity of a SiP***

In terms of power integrity, SiP design also poses challenges. One technique is to share voltage supplies between different chips on the same plane.
Pros: this reduces supply impedance that ameliorates the problem of *simultaneous switched noise* (SSN).
Cons: sharing supplies could create a noise conduit between the different chips. Yet if the supply noise is unacceptable, separate or split planes should be used for the different voltage supplies. These split planes need to be carefully planned so that return paths need to be minimized, which may be difficult because of die stacking.

Overall, electrical design of SiPs becomes complex because of the interactions of different dice and connects to the IC design itself (4).

Electrical Performance - I/O Trends

The electrical requirements depend on the signal speeds and the active and passive components utilized in the SiP.

1. For **servers and communication networks**, a large processor with high I/O count and a large amount of memory may be implemented in a SiP. The die-to-die coupling among stacked-memory ICs and the coupling among bond wires should meet the operating requirement of the memory ICs. The most important requirements, which will be needed, are:
    - a large number of wiring nets with fast rise and fall times in the SiP substrate;
    - a large number of simultaneously switching off-SiP I/Os with fast transition time;
    - impedance of all wiring nets, including vias and I/O leads to the motherboard, should be carefully matched throughout each wiring net;
    - cross-talk noises among adjacent wiring nets should meet the design specification needs;

- voltage and ground planes in the SiP substrate and the leads to the motherboard should meet the simultaneous switching output requirements.

2. For **opto-electronic links,** the most important requirements, which will be needed, are:
    - the extremely fast transition time and high current from the laser driving circuits on the IC to the laser diodes;
    - careful electrical shielding for the receiver section on the SiP substrate;
    - to look into the number of different power rails for noise optimization: adding more rails and keeping well isolated analog power supplies helps reduce noise, coming from signal wiring nets and far-field radiation from other switching nets, but also adds a lot of complexity and cost.
3. The **wireless base station** could have a large number of power amplifiers (PA), one for each active user. The output power of each PA should be carefully regulated according to the distance to its user. When several PAs and the associated control ICs are placed on a SiP, interference among them should be controlled to within the required specification.
4. The SiP for a **cell phone** handset could integrate the baseband digital IC, the memory IC, the up- and down converters, the PA and associated diplexer and filters, plus other passive components. Some of the components could be surface-mounted or embedded in the SiP substrate.
    - The reference planes and vias for the RF section should be carefully isolated from the digital section.
    - The interference between the transmission and receiving paths, including the bond wires, has to meet the specification requirement.
    - some of the passive components and bond wires could be critical elements for the RF section or the phase-lock loop. Their values and placement and the bond wire profile should meet the overall design requirements (4).

4. SiP for Specialized Functions

CPU & Memory

Examples of SiP architectures for CPU and Memory include side by side, stacked die, and embedded die SiP.
Each configuration requires further understanding and defining a set of requirement:

- high bandwidth interconnection schemes, based on considerations which include the number of data lines, interconnect density, data speed, driver power dissipation at CPU and Memory interfaces;
- reduction of the interconnect length to reduce power dissipation and increase data speed;
- good quality power delivery to both the CPU and Memory.

The solution schemes will be dependent on the SiP configuration. Much research is needed for embedded and stacked die configuration (4).

High Power SiP

For industrial applications (power generation, automation, building controls and automotive applications such as hybrid car power devices/systems) the trend is for higher integration of power and power controls to reduce size and improve efficiency. The output power per unit volume and cost per function are the key areas for market success. Innovation will enable highly integrated power modules based on new high power SiP technologies. In the last 5 years this integration has resulted in volume reductions in the range of 60-70% with significant

improvement in energy use efficiency. The introduction of SiP solutions will enable further shrinks in the range of 70-80% with continued improvement in efficiency. This progress depends on continued research in the area of new materials, interconnect technologies, heat dissipation, circuit design, thermal management and modeling and simulation tools (4).

Optoelectronic Components in SiP

The most important requirements for SiP incorporating optoelectronic components are:

- minimal light loss;
- high precision alignment;
- high thermal density associated with many optoelectronic devices;
- good dissipation of heat from high power laser die and high brightness LEDs to maintain the temperature stability during operation and thereby control hot spots in the SiP and minimize wavelength drift of the optoelectronic components (4).

Optical interconnects

The bottleneck to the realization of high-performance microelectronic systems, as SiP, is the lack of low-latency, high-bandwidth, and high density off-chip interconnects.
Some of the challenges in achieving high-bandwidth chip-to-chip communication using electrical interconnects include the high losses in the substrate dielectric, reflections and impedance discontinuities, and susceptibility to cross-talk.
As a result, the use of micro-photonics technology, to overcome these challenges and leverage low-latency and high-bandwidth chip-to-chip communication, seems to be a good solution.
Significant progress has been made in developing chip-to-chip optical interconnects, which include fiber-to-the-chip schemes (in one example, an optical signal is coupled to a silicon-based taper), free-space optical interconnects and guided-wave interconnects.
Some of the optical interconnection technologies are illustrated in the following figure (4).

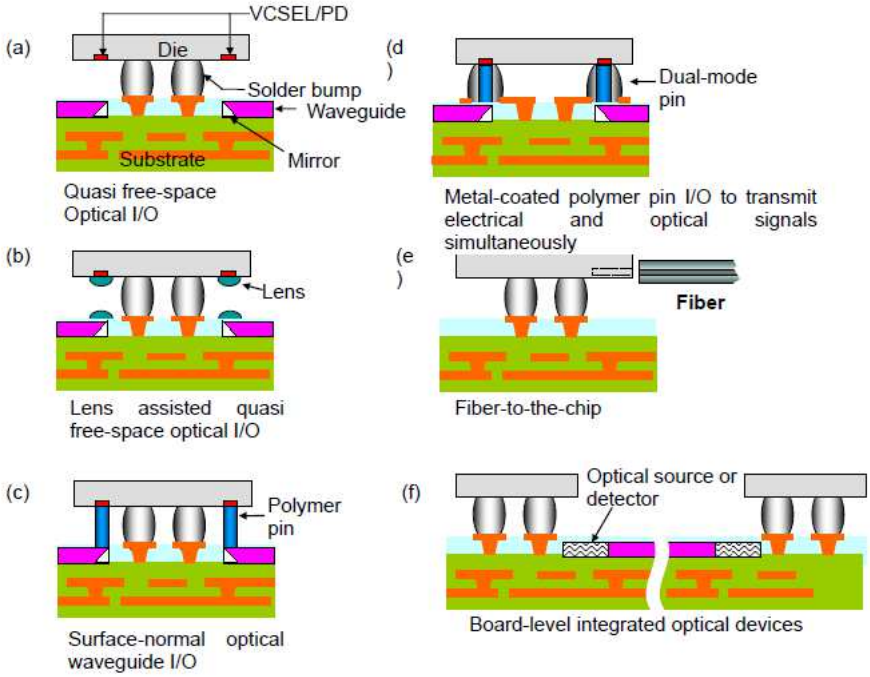


Figure 4-1: Examples of representative guided wave optical interconnects (first level I/O) (4)

These packaging solutions may incorporate chip to chip interconnect within an SiP or provide a long range, high bandwidth communication channel between and SiP and other electronic systems or components.

RF and Millimeter Wave Packaging

Mobile phones are the driver for RF packaging up to a frequency of 5 GHz. Today mobile phones include more and more frequency bands for the various standards like GSM, GPRS, EDGE, UMTS or the new HSDPA (High Speed Downlink Package Access) standard. In addition mobile phones include more and more functionalities like GPS, WLAN, WiFi or Bluetooth, which are related to RF.
Typically the RF part of a mobile phone consists of:

- an RF front-end;
- a transceiver;
- a power amplifier (+ power management) chip including passive components like SAW and BAW filters or RF MEMS.

General trend is higher system integration.
Power amplifiers are especially designed as modules. Some solutions also integrate the power amplifier with the front-end antenna switches in the module.
The main interconnect technology used for RF parts is wire bonding and it is expected that this technology will still be important for the future up to 5 GHz. Flip chip is used for some more complex SiP set-ups (4).

Medical and Bio Chip Packaging

The requirements of medical electronics (biosensors, hearing aids, pacemakers, implantable cardioverter defibrillators and similar products) are often best met with SiP solutions.
The requirements for SiP based medical products are similar to those of SiP based products for other applications with two important exceptions:

1. highest reliability;
2. the environmental requirements of the package have to include exposure to body fluids.

Several areas where additional development is needed for medical SiP are:

- Low power, biocompatible radios with a signal that can reliably penetrate the human body and package to reach a remote receiver.
- Reduced power consumption through improved interconnect.
- Power scavenging from the user's body temperature (up to 30 micro Watts/cm^2) or motion (up to 10 micro Watts/cm^2) to extend battery life of implantable products. This will require research and development of biocompatible MEMS SiP components
- Biological and silicon integration such as neurons grown on silicon. This allows silicon to monitor brain waves to detect seizures and provide counteracting neurostimulus.
- Reliable interoperability of wireless telemetry for medical devices in a world where RF devices operating across a number of frequencies have become ubiquitous (4).

5. SiP Future Trends

SiP is a technology which has the potential to continue the improvement in performance, size, power and cost of electronic system (29).
The future developments in SiP technology will be driven by three principal factors:

1. Time-to-market
2. Functional density
3. Cost-performance

The necessary improvements in SiP functional density will be supported by the wider adoption of flip chip technology for chip-to-chip and chip-to-next-level interconnect, by the greater take-up of IPD networks and TSV technologies. The TSV technology will make a significant move from the present research-and-development mode into SiP product applications over the next few years (30). Recent studies of a 3D-stacked SiP with through silicon via (TSV) interconnections enabled a large number of the shortest signal interconnections through silicon. The advantages of this structure are the smaller form factor, higher data transfer rate, and larger memory size.

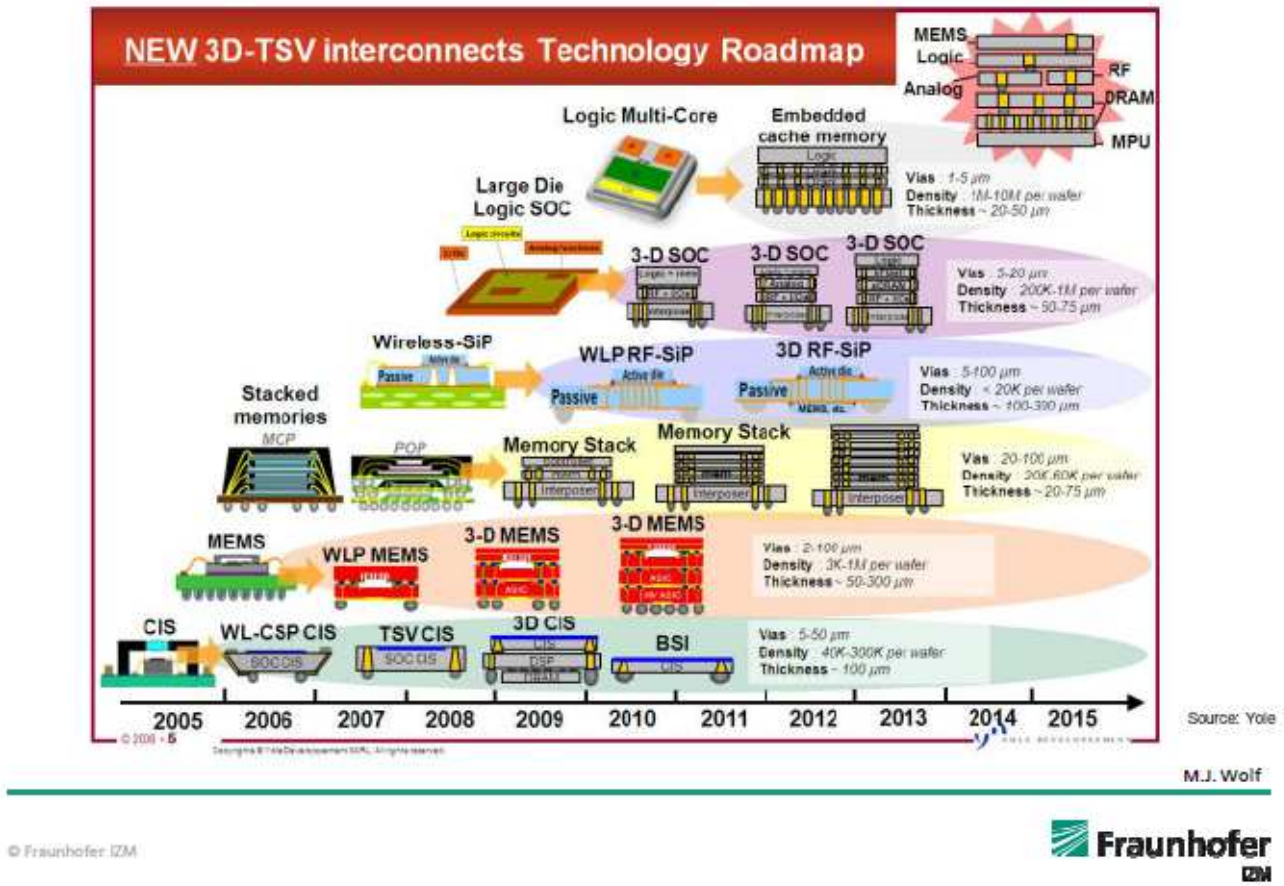


Figure 5-1: 3D TSV interconnects Technology Roadmap (31)

Further specific areas for future SiP technology development are set out in detail in the 2009 iNEMI Roadmap (30):

- the maximum number of die in SiP module is predicted to increase from today's figure of between 6 and 9 to between 8 and 14 by 2014 (depending on application area).
- SiP module I/O counts are predicted to stay fairly level between 2009 and 2014, with typical I/O counts of 200 for RF applications, 800 to 1000 for hand-held and 3000 to 4000 for high-performance products (32)

- the use of TSV structures is predicted to increase from 2 TSV die per module in 2009 to 4 die per module in 2014.
- optical chip-to-chip interconnects within a SiP are likely to gain prominence in the coming years, but integration of wave guides and coupling of wave guides to ICs are major challenges. Multiple research organizations are investigating solutions to switch optical signals within a package, distributing these signals through a 3D die stack, as well as from package to package. Glass substrates have emerged as a strong candidate for such applications (1). In this perspective the benefits offered by plasmonics with respect to traditional photonics would allow having systems at a higher scale of integration, with lower power consumption, and with higher performance in terms of bandwidth thanks to the possibility to aggregate the throughput of multiple channels.

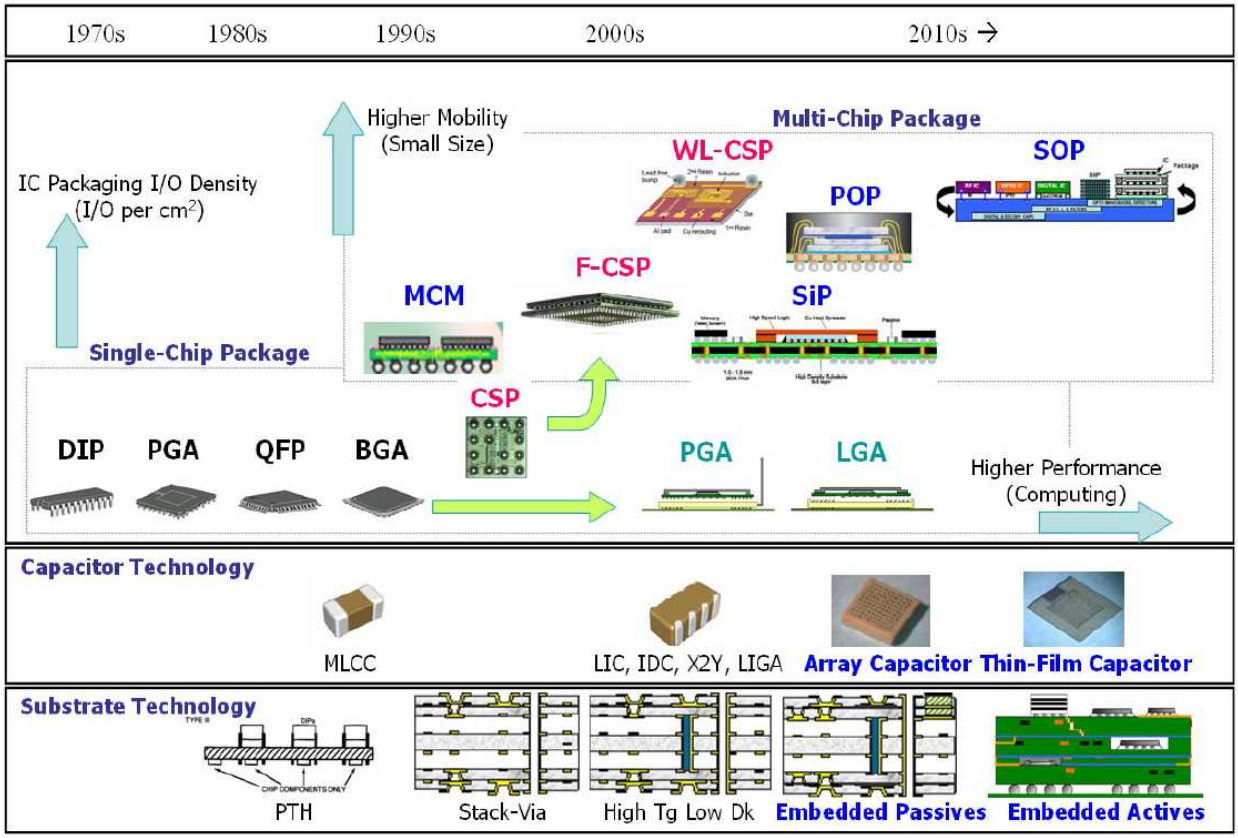
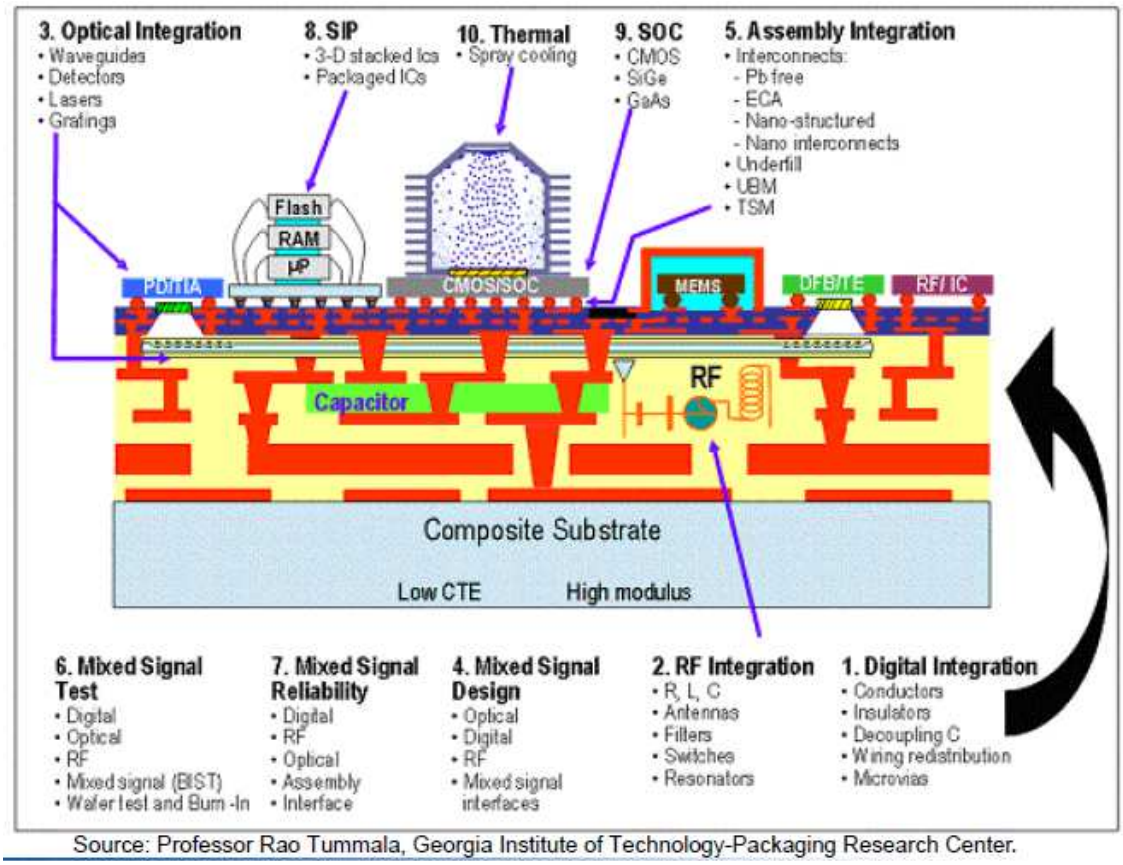


Figure 5-2: Electronic Package Evolution Trends (33)



Source: Professor Rao Tummala, Georgia Institute of Technology-Packaging Research Center.

Figure 5-3: Vision of Evolution of SiP (34)

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