Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Definition of the interconnection level specification employing developed plasmonic components

Milestone no.:	MS4
Due date:	04/30/2013
Actual Submission date:	04/30/2013
Authors:	ST
Work package(s):	WP2
Distribution level:	RE[1] (NAVOLCHI Consortium)
Nature:	document, available online in the restricted area of the NAVOLCHI webpage

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Executive Summary

This document describes the functionality and the microarchitecture of the *PHY adapter* of the Dual Die Communication Module (DDCM) allowing chip-to-chip interconnection exploiting plasmonic devices as components of the physical layer (PHY).

Change Records

Version	Date	Changes	Author
0.1 (draft)	2013-04-30	Start	Alberto Scandurra
1 (submission)	2013-04-30	Final version	Alberto Scandurra

1. *Contents*

1. Introduction

The **Dual Die Communication Module** (abbreviated **DDCM**) is the building-block responsible for the interconnection of different dice within a so called Network in Package (NiP), the communication system enabling inter dice data transmission in the context of Systems in Package (SiP) technology.

According to a widely used approach, the DDCM is seen composed of two main building blocks:

- the DDCM **controller**, responsible for managing incoming/outgoing STNoC/SBus/AMBA-AXI traffic, generating IDN segments through encapsulation and preparing them to be sent to the PHY transmitter, as well as collecting them from the PHY receiver;
- the DDCM **PHY**, responsible for transmitting output phyts across the physical link and collecting inputs phyts from the physical link.

As shown in figure 1.1, the DDCM top level in each die consists of a transmitter (DDCM Tx) and a receiver (DDCM Rx).

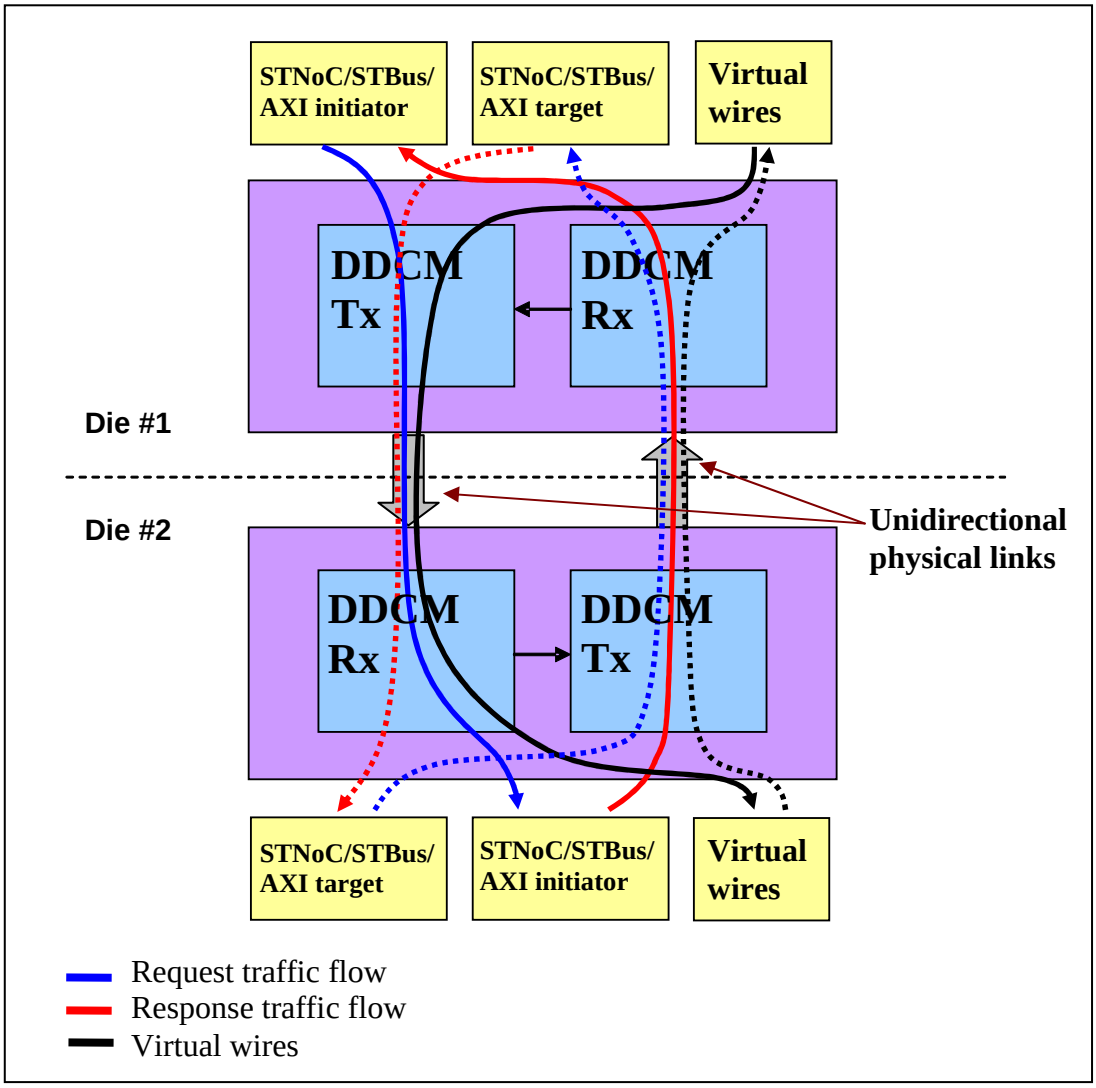

Figure 1-1: DDCM top level architecture and information flow

In such a figure it's possible to see the two information flows supported by a complete DDCM architecture, i.e.

- requests from STNoC/STBus/AMBA-AXI initiators in chip 1 to STNoC/STBus/AMBA-AXI targets in chip 2, responses from STNoC/STBus/AMBA-AXI targets in chip 2 to STNoC/STBus/AMBA-AXI initiators in chip 1, virtual wires from chip 1 to chip 2 (continuous lines);
- requests from STNoC/STBus/AMBA-AXI initiators in chip 2 to STNoC/STBus/AMBA-AXI targets in chip 1, responses from STNoC/STBus/AMBA-AXI targets in chip 1 to STNoC/STBus/AMBA-AXI initiators in chip 2, virtual wires from chip 2 to chip 1 (dotted lines).

Figure 1-2 shows a full architectural view of an DDCM, highlighting the separation between an DDCM transmitter and an DDCM receiver.

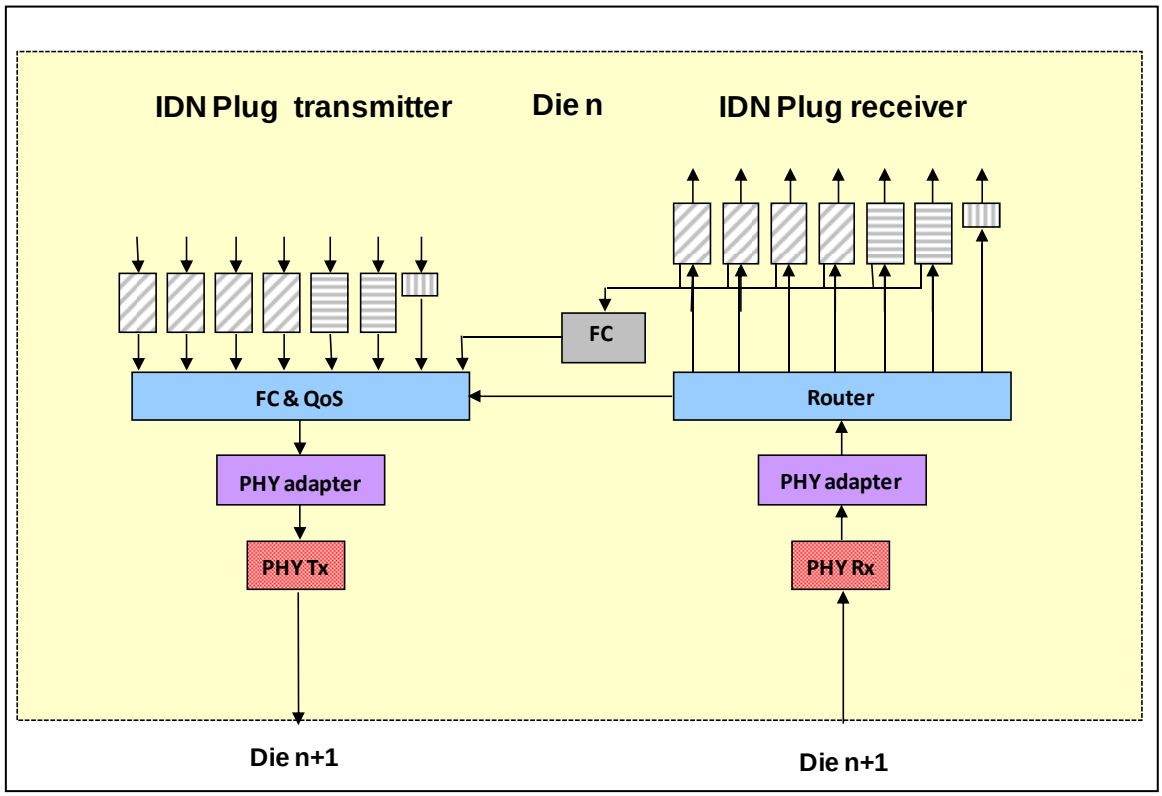

Figure 1-2: DDCM detailed architecture

The next section describes the functionality and the microarchitecture of the PHY adapter intended to exploit the plasmonic devices as physical layer (PHY).

2. DDCM PHY adapter

The DDCM PHY adapter is responsible for adapting the System on Chip (SoC) traffic in such a way to be transferred between the two chips of the system across the physical channel.

Transmitter

The PHY adapter transmitter is responsible for transforming digital data into a format used to modulate the output of the plasmonic LASERs in order to transmit the data across the physical channel (plasmonic waveguide).

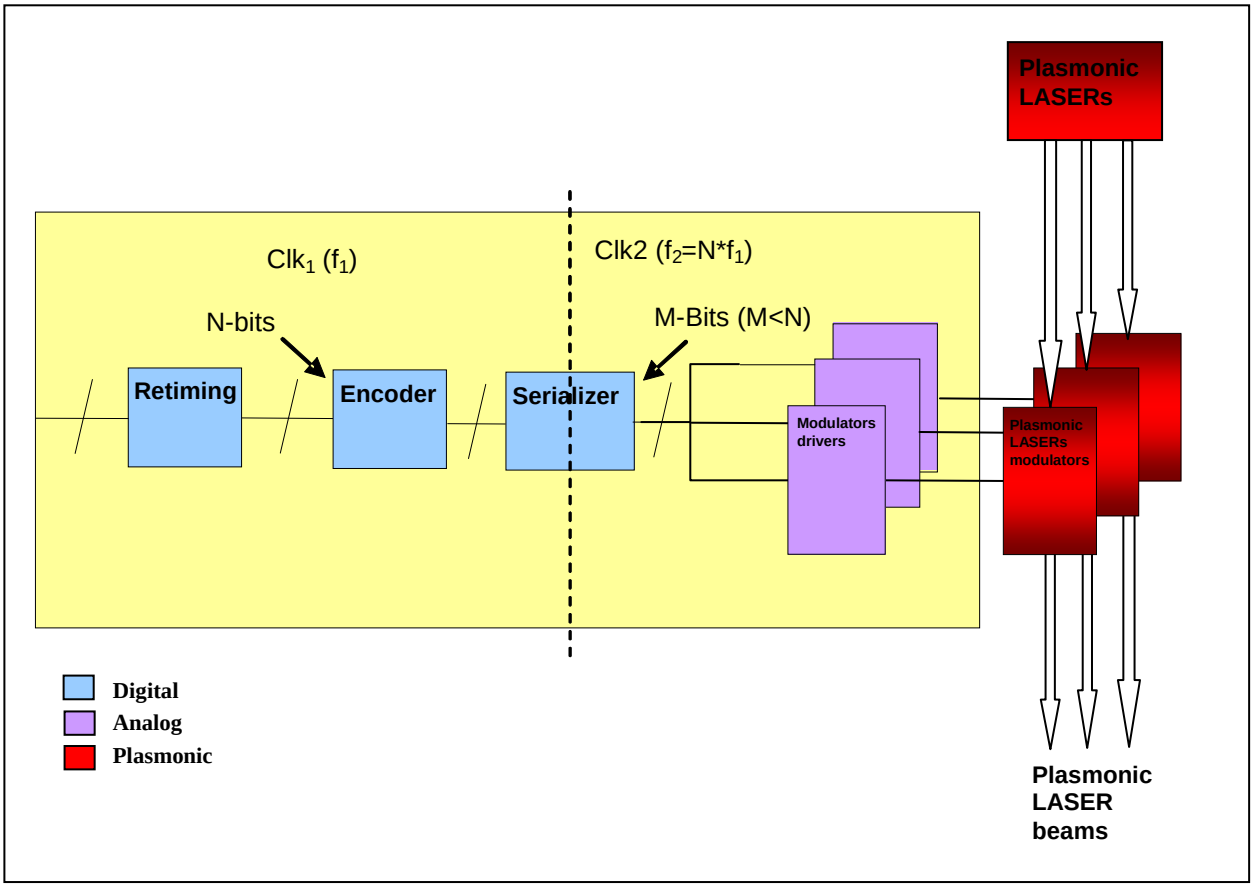

Figure 2-1: PHY adapter transmitter microarchitecture

The PHY adapter transmitter is composed of the following building-blocks:

- a retiming stage;
- a data encoder for power consumption reduction and error detection and correction;
- a serializer to transmit the N-bits data as chunks of M-bits, exploiting the M plasmonic; emitters;
- a set of M modulators, each modulating the output of the related plasmonic LASER.

The **retiming stage** is used as input buffer and for breaking any critical path from the internal parts of the chip-to-chip interface to the PHY adapater components.

The **data encoder** implements source encoding techniques aiming at reducing the dynamic power consumption during data transmission across the physical channel, as well as making the transmitted data immune to noise such as crosstalk or any external corruption.
The **serializer** has the task of breaking the N-bits data into chunks of M-bits, M being the number of plasmonic channels (waveguides) used to transmit the information at physical level.
The outputs of the serializer are used to feed the **drivers** of the plasmonic **modulators**, having the task to modulate the output of the plasmonic LASERs in order to transmit zeros and ones coded as plasmonic signals.

Receiver

The PHY adapter receiver is responsible for the transformation of the plasmonic information got from the physical channel (plasmonic waveguide) into a format suitable to be used by the digital parts of the SoC.

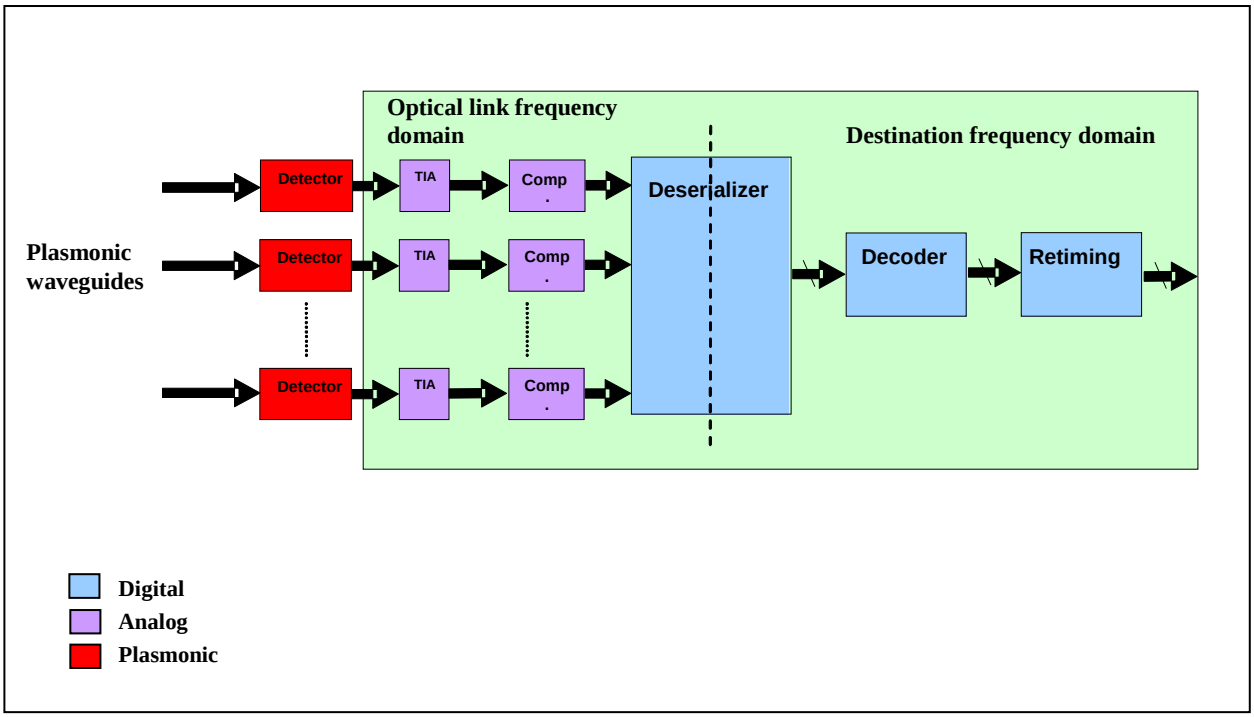

Figure 2-2: PHY adapter receiver microarchitecture

The PHY adapter receiver is composed of the following building-blocks:

- a set of M plasmonic **detectors**, responsible to detect the information transmitted across the asscociated plasmonic waveguide;
- a set of M **Trans-Impedance Amplifiers** (TIA) responsible for translating the output currents generated by the plasmonic photodetectors into voltage levels;
- a set of M voltage **comparators** responsible for associating the proper logic value (‘0‘ or ‘1‘) to the output of the TIAs;
- a **deserializer** to merge the chunks of M-bits, coming from the M plasmonic photodetectors into a N-bits;
- a data **decoder** for power consumption reduction and error detection and correction, counterpart of the encoder in the transmitter;
- a **retiming stage**.

The **plasmonic detectors** are responsible for detecting the plasmonic signals reaching the chip interface across the plasmonic waveguides.
The detectors outputs are converted in CMOS voltage levels by means of **Trans-Impedance Amplifiers**, acting as current to voltage converters, and voltage **comparators**, responsible for giving the voltagse the required levesl in order to be interpreted in the SoC as a zero or one logic values.
The **deserializer** has the task of collecting the chunks of M-bits, M being the number of plasmonic channels (waveguides) used to transmit the information at physical level, into N-bits data used within the SoC.
The data **decoder** implements the counterpart of the source encoder of the PHY adapter transmitter, aiming at reducing the dynamic power consumption during data transmission across the physical channel, as well as making the transmitted data immune to noise such as crosstalk or any external corruption.
The **retiming stage** is used as output buffer and for breaking any critical path from the PHY adapater components to the internal parts of the chip-to-chip interface.