NAVOLCHI 3rd Review Meeting

November 5th 2014, Brussels

FP7-ICT-2011-7
GA 288869

Work Package 6: Integration, Characterization & Testing

"Project NAVOLCHI"

Claudia Hoessbacher, Juerg Leuthold
ETH Zurich, Switzerland

Nano Scale Disruptive Silicon-Plasmonic Platform
for Chip-to-Chip Interconnection

www.navolchi.eu

Outline

1. WP6 Position in Project
2. Objectives
3. Tasks
4. Milestones and Deliverables
5. Status of Work

   Task 6.1 Characterization of active and passive plasmonic devices

   Task 6.2 Assembly and packaging of plasmonic devices into System in Package

   Interconnect System – Contincengy Plan
6. Summary and Outlook

WP6 Position in Project

SEVENTH FRAMEWORK PROGRAMME

WP1 [KIT]

Project Managment

WP2 [AIT]

Definition and specifications of plasmonic chip-to-chip interconnection platform

WP3 [TUE]

Plasmonic Transmitter

WP4 [UV]

Plasmonic Receiver

WP5 [IMEC]

Optical and electrical interfaces for plasmonic interconnection platform

WP6 [ST]

Integration, Characterization & Testing

WP7 [AIT]

Exploitation, Dissemination & Publication

Contributors:

Objectives

- Characterization and **testing of** active and passive **plasmonic devices**
- **Integration** of plasmonic devices **with the electrical parts** the chip-to-chip communication structure is composed of
- Characterization and **testing of a complete System in Package**

Tasks

	Names of the Tasks	Time Period [months]
Task 6.1	Characterization of active and passive plasmonic devices	7 – 33
Task 6.2	Assembly and packaging of plasmonic devices into System in Package	30 – 36
Task 6.3	Plasmonic chip to chip interconnect prototype testing and evaluation	32 – 36 → 45
Task 6.4	System-in-Package integration and characterization	22 – 36 → 45

Milestones

SEVENTH FRAMEWORK PROGRAMME

	Names of the Milestones	Month	Partner
MS37	Plasmonic active device characterization results	12	KIT
MS38	Plasmonic passive components characterization results with a 1dB coupling loss	24	KIT
MS39	Concept for system integration developed	27	AIT
MS40	Individual plasmonic devices characteriaztion, testing and evaluation	30 → 39	TU/e
MS41	Chip to chip interconnect characterization	33 → 42	ST
MS42	Plasmonic components integration to demonstrate chip-to-chip interconnect	33 → 42	AIT
MS43	Plasmonic chip to chip interconnect prototype testing and evaluation	36 → 45	ST

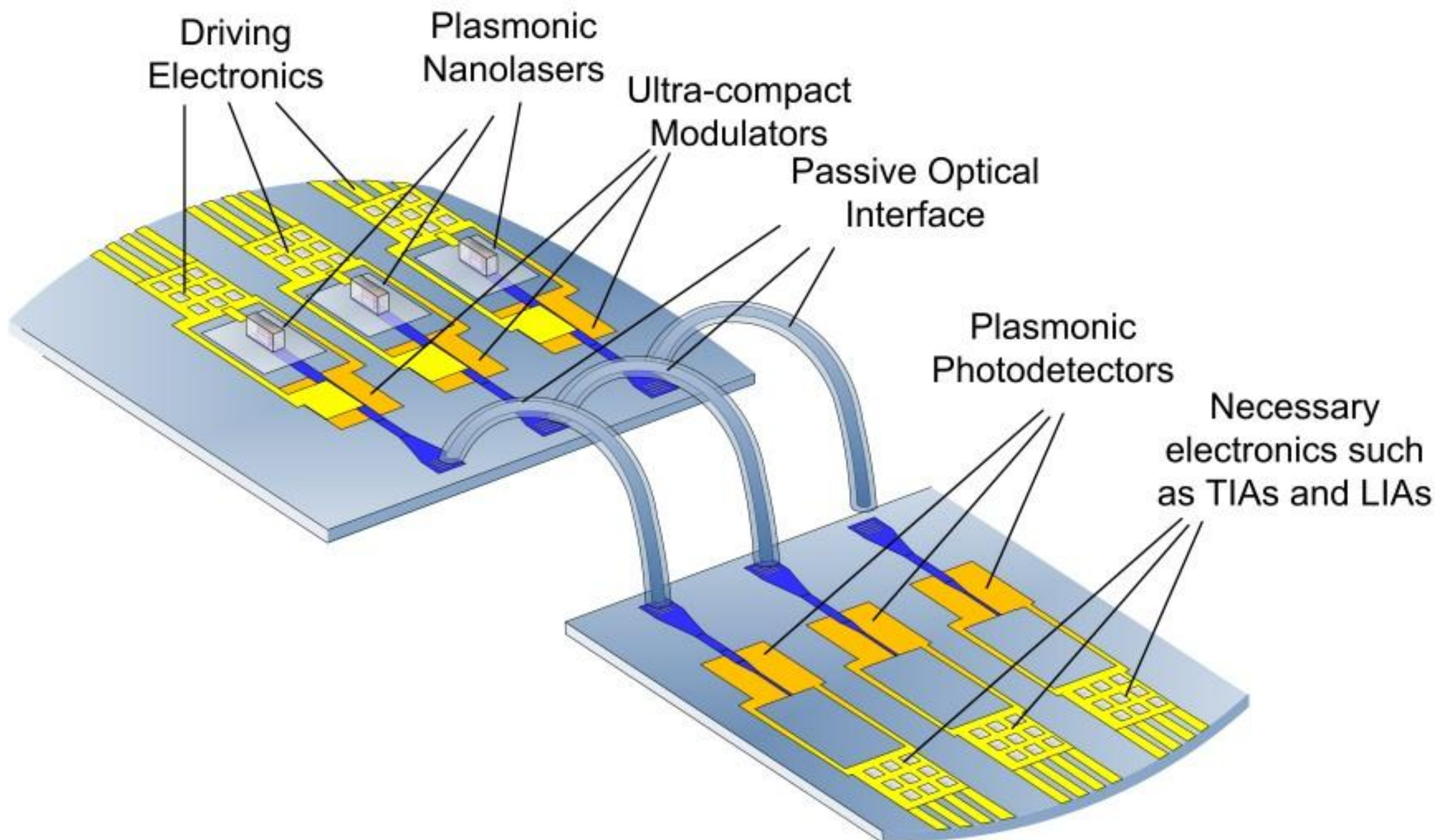
Deliverables

SEVENTH FRAMEWORK PROGRAMME

	Names of the Deliverables	Month	Partner
D6.1	Report on characterization results of all plasmonic devices	(27) 36	TU/e
D6.2	Report on characterization results of all optical interface plasmonic passive components	(27) 36	KIT
D6.3	Report on chip to chip interconnect characterization	36 → 45	ETH
D6.4	Report on plasmonic chip-to-chip interconnect prototype testing and evaluation	36 → 45	AIT

WP6: Assembly to Plasmonic Chip-to-Chip Interconnect Array

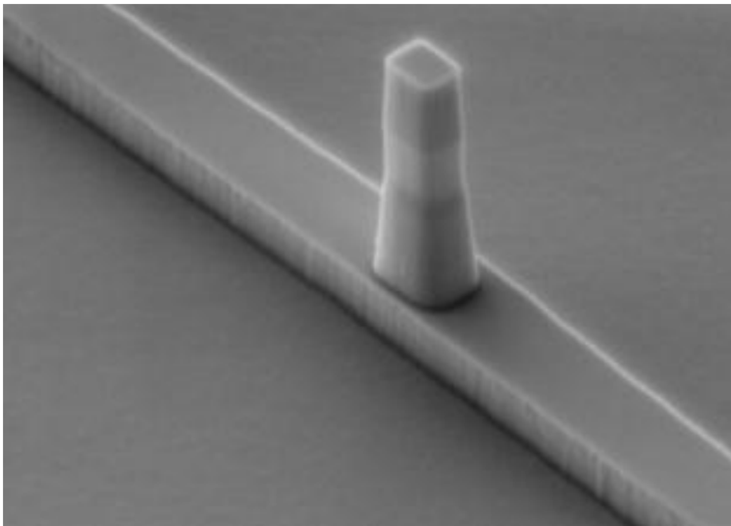
SEVENTH FRAMEWORK PROGRAMME



Task 6.1 Characterization of Active and Passive Plasmonic Devices

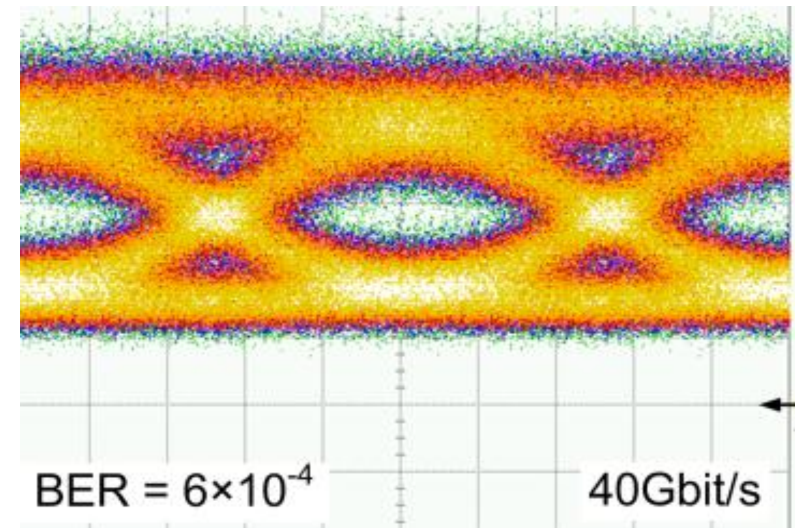
SEVENTH FRAMEWORK PROGRAMME

Laser



- Fabrication process of III-V laser on silicon fully developd
- Characterization beginning of next year

Mach-Zehnder Modulator

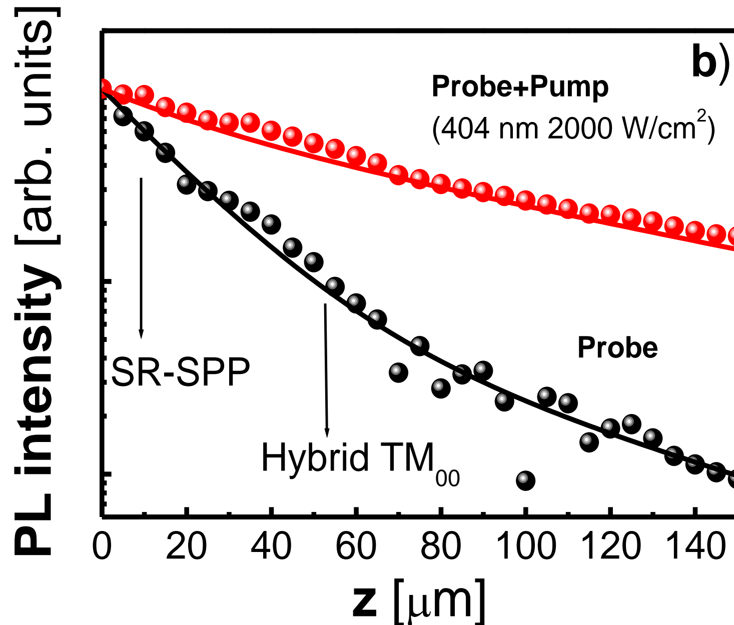


- Data rates: 40 Gbit/s (BER 6×10^{-4})
- Energy consumption: 75…225 fJ/bit
- Device length: 29 µm
- Loss: 12 dB

Task 6.1 Characterization of Active and Passive Plasmonic Devices

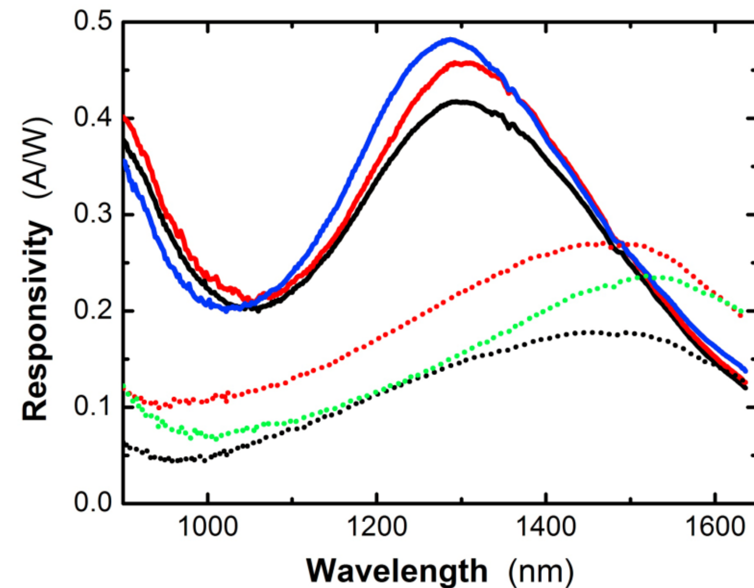
SEVENTH FRAMEWORK PROGRAMME

Amplifier



- @1550 nm: compensation of losses, no gain yet
- Outlook: gain by using HgTe QDs in dielectric matrix

Photodetector

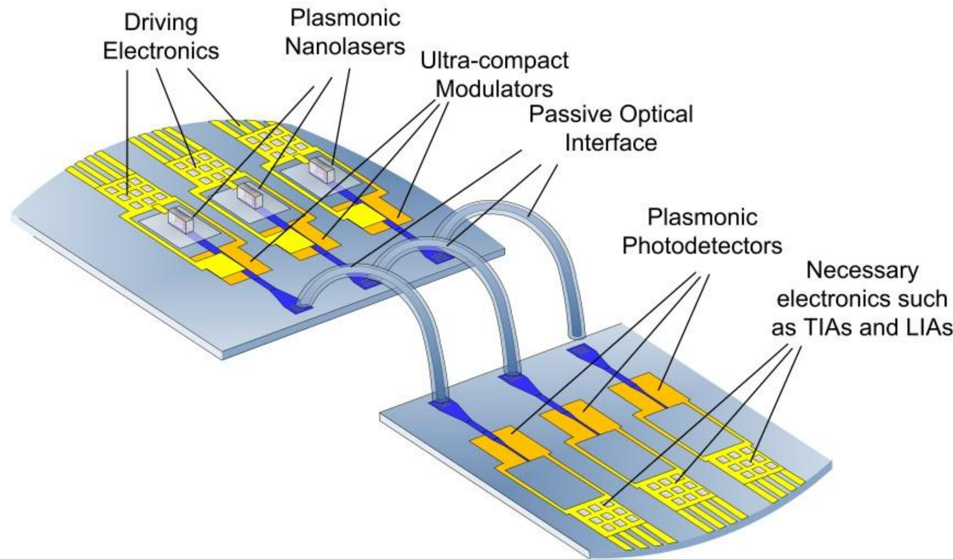


- Schottky:
  - Responsivity: 0.1-0.3 A/W
  - Speed limited
- Outlook: Nano-gap PDs

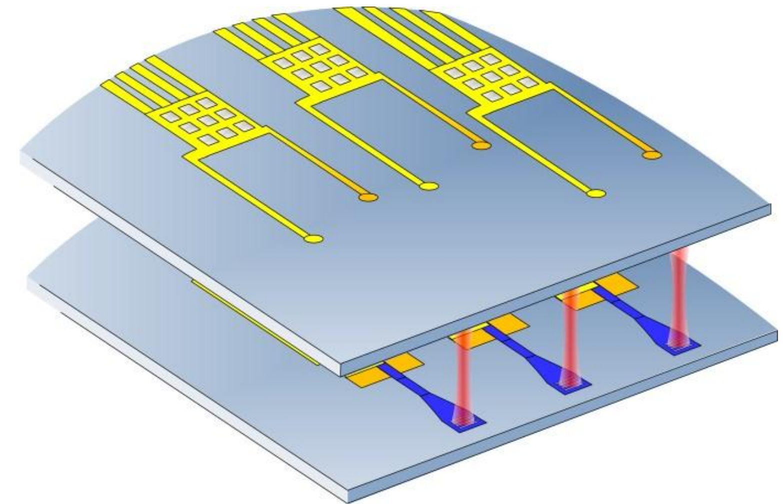
Task 6.2 Assembly and Packaging of Plasmonic Devices into System in Package

SEVENTH FRAMEWORK PROGRAMME

2D in-plane packaging



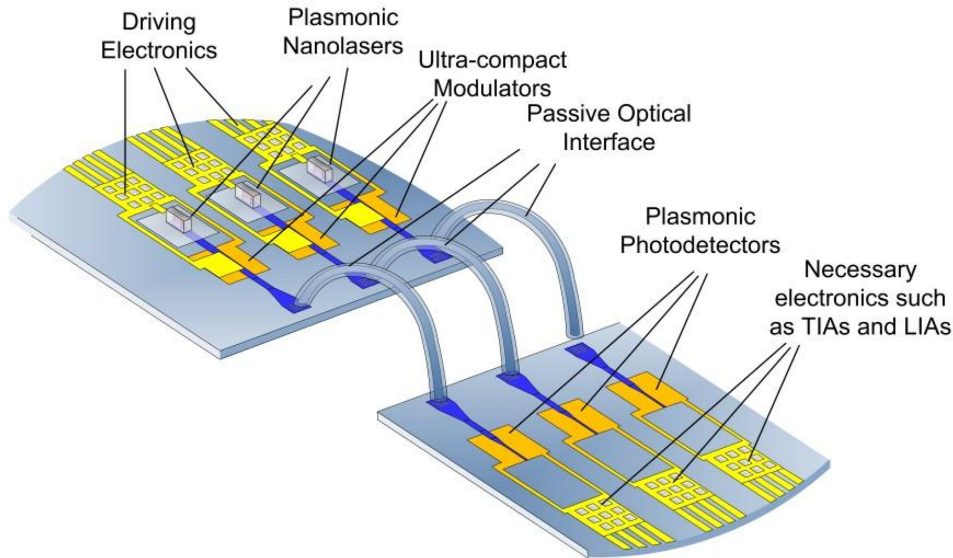
3D vertical stacking



Task 6.2 Assembly and Packaging of Plasmonic Devices into System in Package

SEVENTH FRAMEWORK PROGRAMME

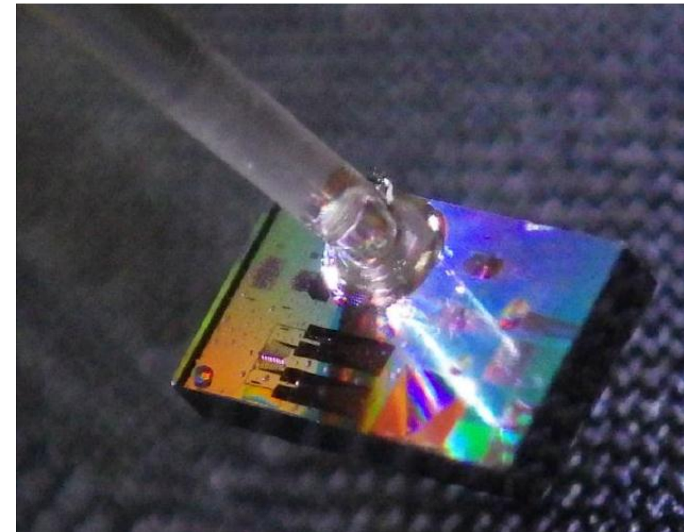
2D in-plane packaging



Advantages

- 4 channels with 50 μm pitch
- Interchannel coupling <-35 dB
- No additional fabrication steps
- Allows for additional optical amplifier

Commercial fiber arrays (Chiral Photonics)

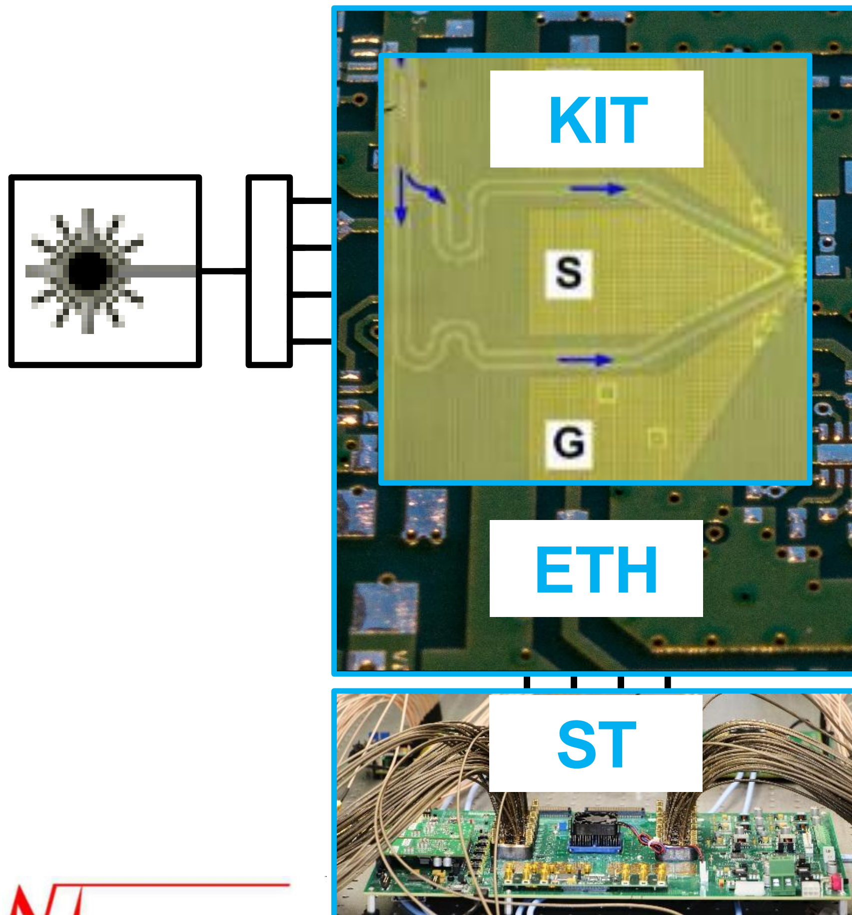


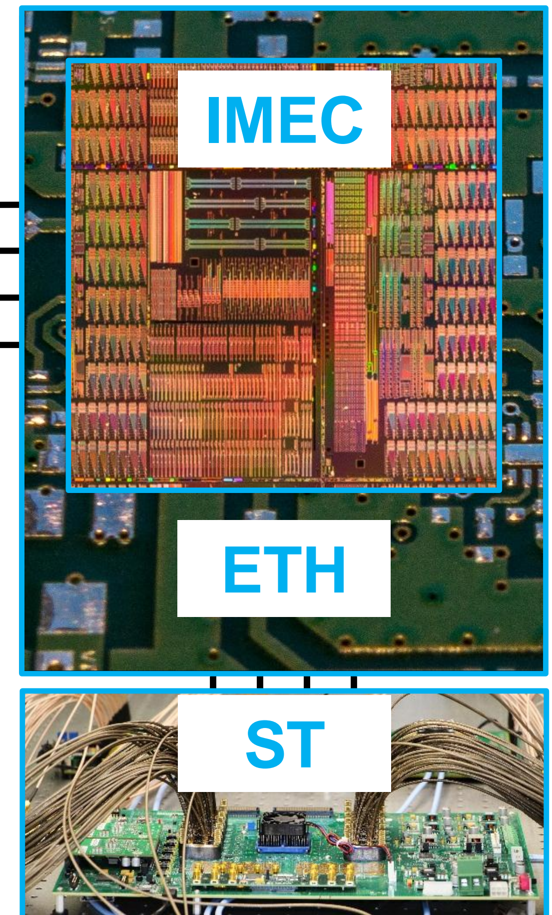
[1]

[1] V. I. Kopp, J. Park, M. S. Wlodawski, E. Hubner, J. Singer, D. Neugroschl, *et al.*, *Two-dimensional, 37-channel, high-bandwidth, ultra-dense silicon photonics optical interface*, 2014.

Interconnect System – Contingency Plan

SEVENTH FRAMEWORK PROGRAMME



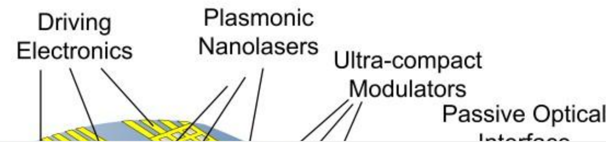


Interconnect System – Contingency Plan

SEVENTH FRAMEWORK PROGRAMME

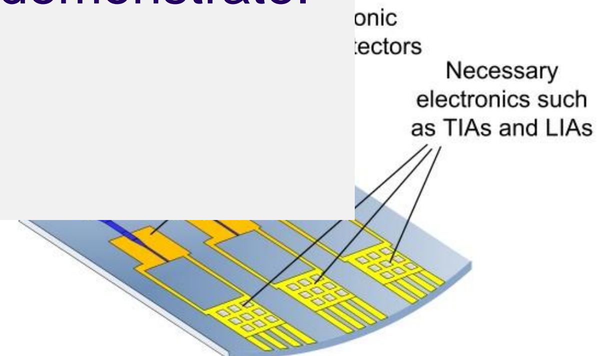
System Level Specifications Transmitter

- 4 optical channels with 50 µm pitch (modulator length: 29 µm)
- Data rate: 40 Gbit/s
- Optical bandwidth: 120 nm
- Energy consumption modulator: 75 fJ/bit
- Insertion loss: 12 dB



NAVOLCHI interconnect system will demonstrate:

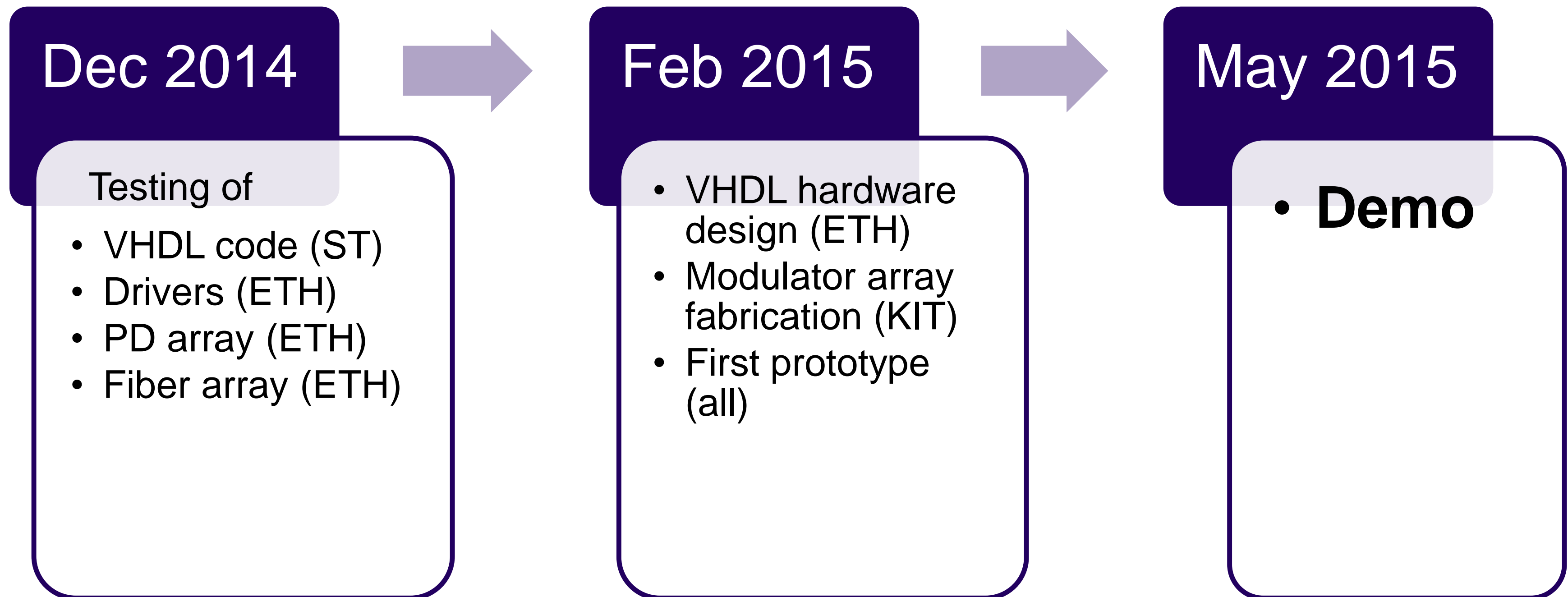
- Small footprint
- High speed
- Broadband operation



Interconnect System – Contingency Plan

SEVENTH FRAMEWORK PROGRAMME

Timeline



Summary and Outlook

- **Summary**
  - Progress in characterization of active and passive plasmonic devices
  - Integration of plasmonic devices with the electrical parts started
- **Outlook**
  - Complete integration of plasmonic devices with the electrical parts
  - Characterization and testing of a complete System in Package