



## Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

### Fabrication of plasmonic waveguide couplers with less than 3 dB coupling loss

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#### List of Partners concerned

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### *Executive Summary*

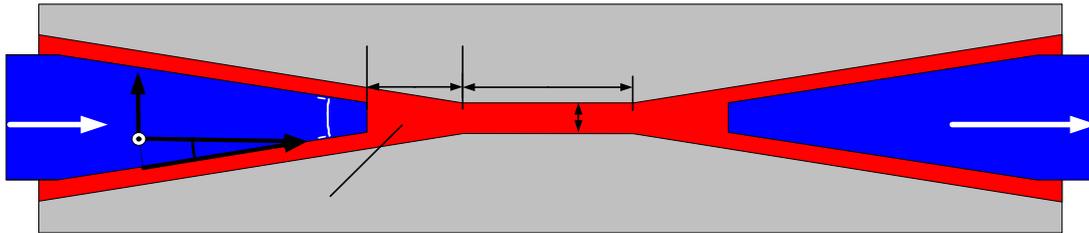
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### *Change Records*

| Version        | Date       | Changes | Author            |
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| 0.1 (draft)    | 2012-11-12 | Start   | Argishti Melikyan |
| 1 (submission) | 2012-11-12 |         | Argishti Melikyan |

## Introduction

It has been shown in the Milestones 9 and in the Deliverable 3.2 that the figure of merits of the plasmonic modulators are dramatically increasing while reducing the size of the plasmonic slot below 100nm. However, the excitation of the surface plasmon polariton in the metallic nanoslots with these dimensions is challenging and requires special care in the design of the coupling structure. We employ metallic tapered coupling structure which we have optimized for its highest transmission in in the case of given geometrical and material properties. Less than 1dB coupling losses are theoretically estimated for the optimized couplers.

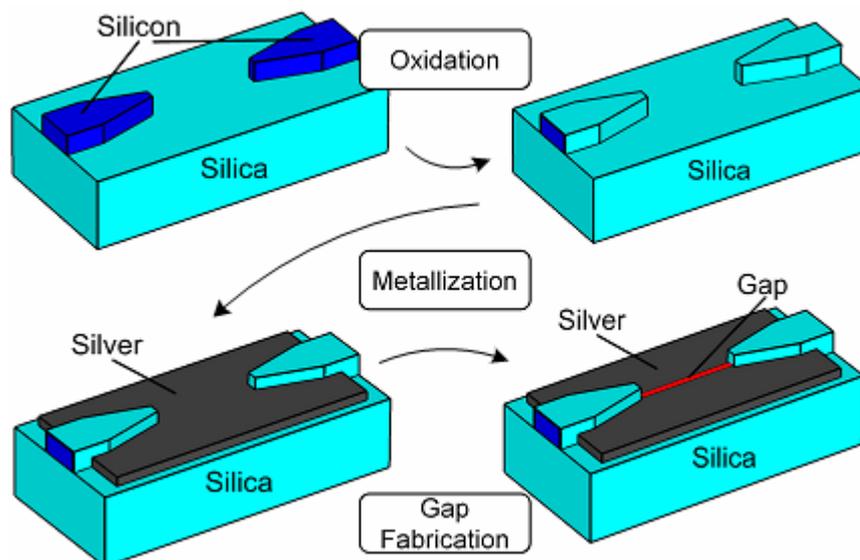


**Figure 1 Top view of the SPP coupling structure. Light guided through silicon nanowire is adiabatically squeezed and launched into metallic nano-slot.**

In this milestone, we discuss the work progress in developing efficient couplers for the excitation of surface plasmon polaritons in the metallic nanoslots. We describe the process flows employed and the initial characterization results of the couplers

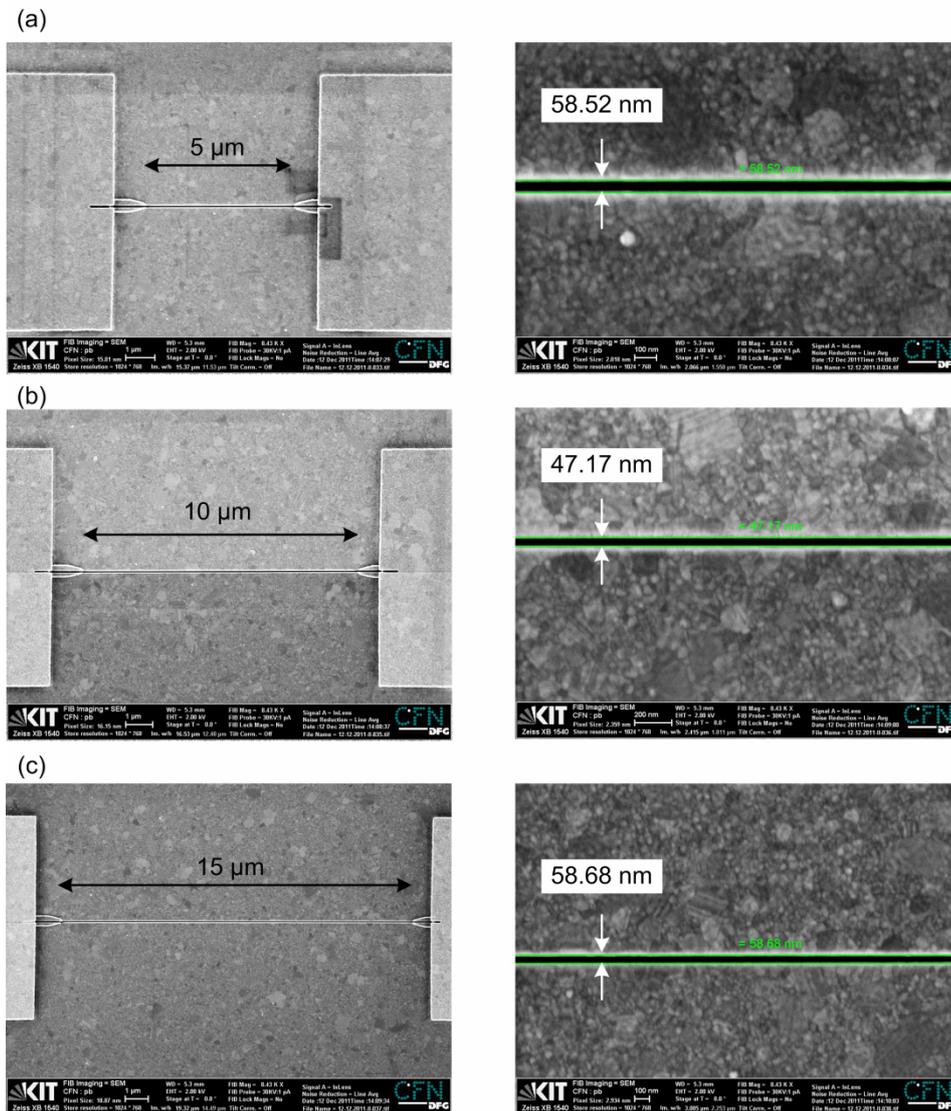
## Methods and Results

Silicon part of the entire coupler first has been design by KIT based on the previous optimized geometry discussed in Milestone 25. IMEC has processed an entire SOI wafer with a top silicon device thickness of 220nm using the design layout provided by KIT. The wafer has been diced at IMEC and shipped to KIT, where the post processing of the diced samples has been carried out to design the metallic part of the couplers. The entire process flow for the fabrication of metallic tapered couplers as well as of the modulators is depicted in Fig. 2. The silicon waveguide first



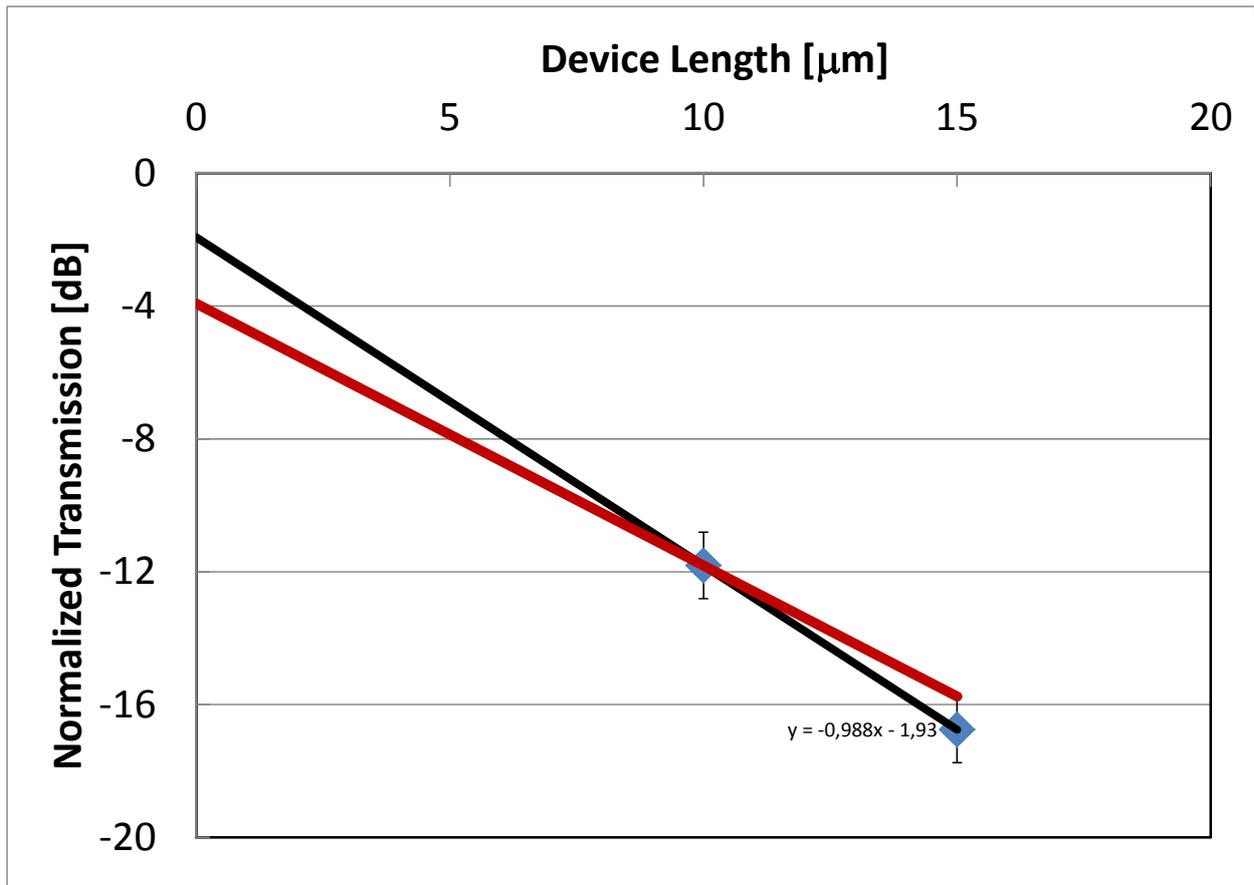
**Figure 2 Process flow for fabrication of the plasmonic phase modulator**





**Figure 5 SEM images of fabricated couplers before stripping. All milled slots are perfectly hit in the middle of the tips with narrow slots of 47 nm and 58 nm. Images in the same row correspond to each other.**





**Figure 7** The insertion loss of the couplers with different separations of 10 $\mu\text{m}$  and 15 $\mu\text{m}$ . The coupling loss can be calculated by linear interpolation towards zero separation. Linear interpolation from the measurement points obtained from 120nm and 167nm slot widths (black line). Linear interpolation from the points taking into the different propagation lengths of the plasmonic waveguides with 120nm and 167nm slot widths (red line).

In conclusion, KIT with the help of IMEC has completed the first run of the fabrication and characterization of the plasmonic couplers. About 2dB coupling loss is measured for the plasmonic couplers fabricated with the lift off approach. The second fabrication run for the plasmonic modulator various length is in progress.