



Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

M51 – Report on enhanced metal grating couplers

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Executive Summary

This report describes the results on a new kind of metal grating couplers. This new device was not originally planned within NAVOLCHI, however it was identified to be relevant for the project and therefore it was developed in parallel. Here, we present the device design, propose and validate a fabrication process and show characterization results. The device shows a chip-to-fiber coupling efficiency of 56% and a 3dB-bandwidth of 61nm for a uniform grating coupler.

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1. Introduction

Integrated photonic platforms using a semiconductor membrane have gained much interest in recent years. Among their advantages are very compact devices leading to a higher integration density and potentially better energy efficiency.

In the membrane-based platforms grating couplers are required for photonic integrated circuits (PICs), as they allow alignment tolerant mode matching from the compact photonic wires to a fiber and can be placed in high density anywhere on a chip. For a number of applications like on-wafer characterization or optical interconnects systems [1-3] chip-to-fiber couplers with high efficiency, broad spectral response and high yield fabrication are essential. However, present grating designs have performance limitations, since the light is diffracted both downwards and upwards from the photonic membrane. A high efficiency is, therefore, only achievable with a tight control of the buffer thickness that allows constructive interference of the diffracted light [4,6]. Additionally, power leaking to the substrate may cause undesired crosstalk.

To overcome these drawbacks, different types of gratings have been designed. Among them, the design of P.Lin in 2012, which shows a coupling efficiency independent from the buffer thickness [6]; however, it makes use of a 600nm thick metal grating with 305nm wide slots which is very challenging to fabricate..

2. Design

We recently proposed a metallic grating coupler for TE polarization that consists of a metal grating, formed with buried stripes patterned in SiO_x and a metal mirror layer [7,8]. A schematic representation of the device is shown in Fig. 1.

The grating is designed to couple light of a wavelength of $\lambda = 1.55\mu\text{m}$ to a single mode fiber (SMF) with $9\mu\text{m}$ core diameter. The grating has a periodicity of $\Lambda = 635\text{nm}$ and depth of $d = 125\text{nm}$ in the SiO_x layer. The InP wave-guiding layer has a thickness of 300nm and a footprint of $16 \times 25\mu\text{m}^2$ in the metal grating area. The grating is connected to a 400nm wide waveguide via a linear taper with a length of $250\mu\text{m}$. The fabrication is compatible with bonded SOI [5] and InP-membranes [9]. Moreover, it results in a highly efficient grating coupler, that is independent from the buffer thickness, inhibits power leakage into the substrate and makes use of standard fabrication processes [7]. A high flexibility in the buffer layer thickness can be of advantage in a variety of applications: a thin bonding layer is, for example, necessary for heterogeneous integration when connecting SOI circuits to III-V gain-materials [10]. A thick bonding layer, on the other hand could be useful for thermal isolation between a photonic membrane and an underlying CMOS circuit.

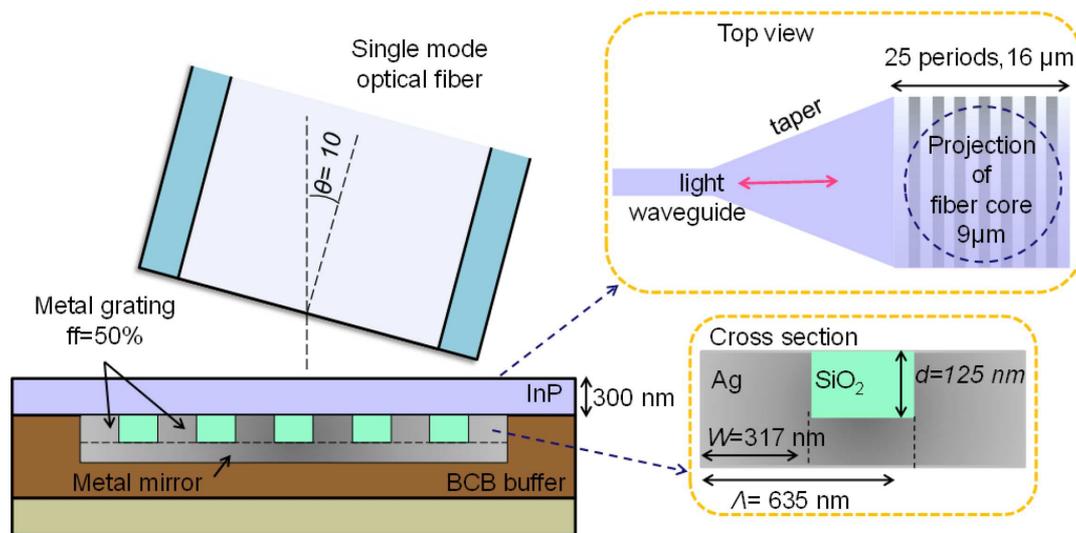


Fig. 1. Schematic of the buried metal grating design.

Our grating design was simulated using 2D finite difference time domain (FDTD) calculations. The results show a diffraction to free space with an efficiency of 84% or, up to 70% efficiency when coupling to a single mode fiber located at 10° and $10\mu m$ vertical distance from the grating. Note, that the fiber coupling efficiency can be further increased up to 84% by adding apodization schemes to the grating design.

3. Fabrication

The metal grating couplers are defined in a thin III-V membrane bonded to a silicon wafer. The design of the grating couplers requires processing on both sides of the membrane. Therefore, we firstly define the gratings on the III-V wafer. After adhesive bonding to a Si wafer [10] the waveguides are etched in the thin InP membrane.

In a first electron beam lithography (EBL) step we pattern the alignment markers used for the further overlay exposures. We use positive resist ZEP520A with a thickness of 320nm on top of a 300nm thick SiNx hard mask. The pattern is transferred from the resist to the SiNx by reactive ion etching (RIE). Afterwards we etch the semiconductor layers 690nm deep by inductive coupling plasma (ICP) with methane hydrogen ($CH_4:H_2$) chemistry at $60^\circ C$.

To define the grating we first pattern stripes in SiOx, as schematically depicted in Fig. 2a. We deposit a layer of 125nm thick SiOx using Plasma Enhanced Chemical Vapor Deposition (PECVD). Using a second EBL step with ZEP520A we define the stripe pattern with a pitch of 635nm and a filling factor of 50%, which is etched via RIE using pure CHF_3 chemistry. Fig. 2a shows a scanning electron microscopy (SEM) picture of the SiOx pattern. We observe the oxide floor and a good pattern definition.

In the next fabrication step we cover the oxide stripes with Silver (Fig. 2b). After a third EBL step using 800nm thick PMMA495A11 we deposit a layer of 2nm germanium to improve adhesion followed by a 300nm thick layer of silver. These layers are deposited in an electron beam evaporator in a single step recipe, without breaking the vacuum. Figure 2b shows an SEM picture of cross-section through the grating after a focused ion beam cut (FIB). The oxide grating

is fully covered with the thick metal layer. In previous trials we deposited germanium and silver in different machines, exposing the sample to air in between. The single step method showed an increased grain size, improved uniformity and lower optical losses in the metal layer.

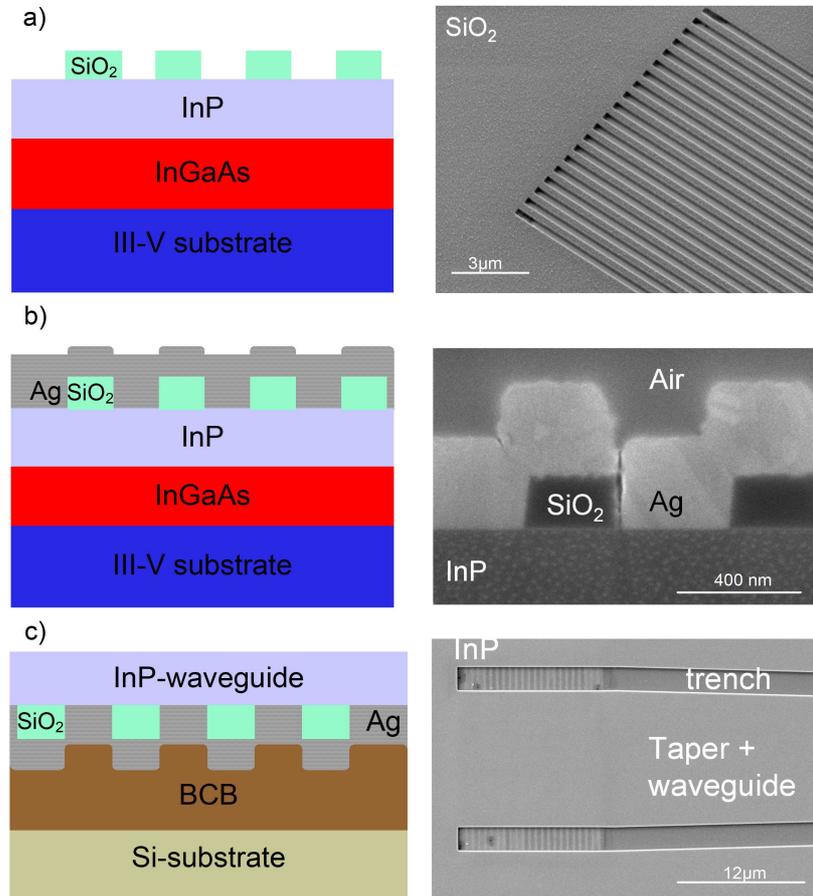


Fig. 2. a) 2nd EBL step: cross-section of the SiOx pattern, b) FIB cross-section of the metal grating before bonding and c), 4th EBL step, cross-section of the bonding and top view SEM picture of the fabricated metal gratings.

After silver deposition, the chip is bonded to a silicon substrate using a benzocyclobutene (BCB) layer as adhesive. Here, the Si wafer and III-V chip are prepared as follows: a 3" Si wafer is cleaned and 1000nm of SiOx are deposited as optical buffer layer between the InP membrane and the Silicon substrate. Then, a BCB layer with a thickness between 600 to 900 nm is spun on the Si wafer. Note that the thickness of the spun BCB is not controlled carefully, as the simulated performance of the gratings is independent of the buffer thickness [7,8]. Then, we cure the BCB partially by heating the sample to 180°C inside a vacuum oven for 1hr. Meanwhile, 100nm of SiOx are deposited on the III-V chip to promote adhesion to the BCB. After the curing, the III-V chip is placed epi-side down on the silicon wafer and is introduced into a bonding machine with an specific compressive force of 25N/cm² and 180°C for 1hr. Finally, the InP substrate of the III-V chip is removed with HCl:H₂O for 30 minutes. As indicated in Fig. 2c, the metal gratings are now buried under the 300nm thick InP-membrane, which can be patterned with waveguides.

This is done in a third EBL, where we pattern 2.5μm wide trenches in the positive resist ZEP 520A to define the waveguides, which are typically 400nm wide. We use 100nm of SiNx as hard mask. Nitride RIE and ICP steps are performed to transfer the pattern 250nm deep into the InP

membrane. This leaves a footing of 50nm on the InP membrane to avoid exposing the oxide or BCB layer which would be attacked by HF when removing the SiNx hard mask.

4. Characterization

After fabrication we characterize the grating losses with a vertical coupling setup, which is schematically depicted in the inset of Fig. 3a. We use two SMFs which are vertically positioned to couple light in and out of the gratings and are aligned to a 10° angle with respect to the vertical axis. The input fiber is connected to a tunable laser via a polarization maintaining SMF and a fiber polarization controller. The vertical distance to the fiber as well as movement in the sample plane can be accurately controlled with nanometer step stages. The output SMF is connected to an InGaAs detector. The devices under test consist of two metallic grating couplers with $250\mu\text{m}$ long tapers back to back.

The total insertion loss considers the grating, a taper and the connectors. Figure 3a shows the transmission spectra obtained for five different devices after correcting for the system response. The ripples in the spectral response can be attributed to weak reflections at the grating couplers.

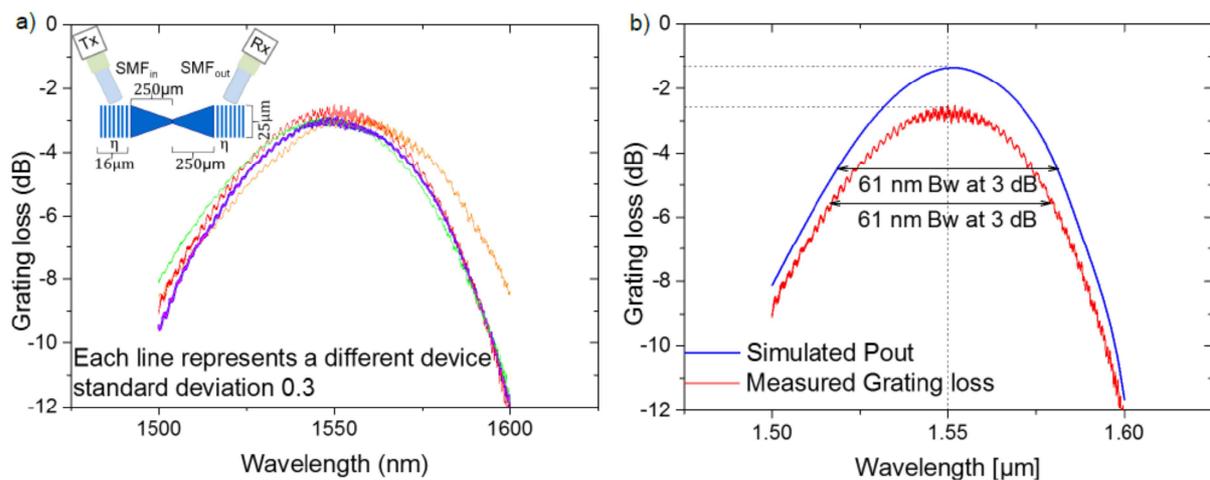


Fig. 3. a) Grating loss versus wavelength and schematic of devices under test (Tx represents the laser, Rx represents the detector). b) Comparison of the grating loss versus wavelength of the simulated performance and best case of the characterized devices.

The best grating coupler (red line) shows a single grating loss of 2.5dB that corresponds to 56% of efficiency and a 3dB bandwidth of 61nm.

In Fig. 3b the simulated transmission previously published in [7] is plotted in addition to the experimental data. The simulated grating loss is only 1.5dB smaller than the experimental one. We attribute this partly to an increased loss due to metal absorption. The values used in the simulations [11] are only achievable under ideal conditions, including high temperature annealing, which could not be performed in our device. Moreover, the tapers which are included in the loss figure are designed to be lossless. Nevertheless, the quality of the wafer bonding, as well as the sidewall roughness introduced by the etch step will lead to additional scattering losses.

5. Conclusions

This article presents a novel design for non-apodized membrane-based coupling grating for integrated photonics. In contrast to other designs its performance is independent of the buffer thickness, it uses standard fabrication processes with high yield, and parasitic leakage of light to the substrate is strongly reduced. The gratings show a wide 3dB-bandwidth of 61nm and high efficiencies of up to 56%. The design presented here uses uniform gratings and linear tapers. In an apodized design a higher coupling efficiency up to 84% coupled to a fiber could be achieved [7]. Its unique properties could be useful in a wide range of integrated photonic circuits.

6. References

- [1] Hofrichter, J., Green, W.M.J., Horst, F., Assefa, S., Yang, M., Offrein, B., and Vlasov, Y. (2011). "Grating couplers as optical probe pads in a standard CMOS process." 8th IEEE International Conference on Group IV Photonics, 127-129.
- [2] Zheng, X., and Krishnamoorthy, A. V. (2011). "Si photonics technology for future optical interconnection." Proc. SPIE 8309, Optical Transmission Systems, Subsystems, and Technologies IX, 8309, 83091V.
- [3] Atsumi, Y., Sifer, T., Kang, J., Hayashi, Y., Nishiyama, N., and Arai, S. (2013). "Ultraviolet-induced wavelength trimming of BCB-buried athermal Si slot wavelength filters." Pacific Rim Conference on Lasers and Electro-Optics, CLEO - Technical Digest, 2–3.
- [4] Roelkens, G., Van Thourhout, D., and Baets, R. (2006). "High efficiency Silicon-on-Insulator grating coupler based on a poly-Silicon overlay." Optics Express, 14(24), 11622.
- [5] Laere, F. Van, Roelkens, G., Ayre, M., Schrauwen, J., Taillaert, D., Thourhout, D. Van, , Baets, R. (2007). "Compact and Highly Efficient Grating Couplers Between Optical Fiber and Nanophotonic Waveguides," 25(1), 151-156.
- [6] Lin, P.T., Wu, C.Y., and Lee, P.T. (2012). "Buried metal grating for vertical fiber-waveguide coupling with high directionality. Advanced Photonics Congress," 1(c), IM4B.6.
- [7] Dolores-Calzadilla, V., Heiss, D., and Smit, M. (2014). "Highly efficient metal grating coupler for membrane-based integrated photonics." Optics Letters, 39.
- [8] Dolores-Calzadilla, V., Heiss, D., and Smit, M. (2014). "Highly efficient metal grating coupler for membrane-based integrated photonics." In IPR.
- [9] Van der Tol, J., Zhang, R., Pello, J., Bordas, F., Roelkens, G., Ambrosius, H., ...Smit, M. (2011). "Photonic integration in indium-phosphide membranes on silicon. IET Optoelectronics," 5(5), 218-225.

[10] Roelkens, G., Thourhout, V. D., Christiaens, I., Baets, R., and Smit, M. K. (2005). "Ultra thin BCB bonding for heterogeneous integration of III-V devices and SOI photonic components." In 12th European conference on integrated optics. Grenoble.

[11] Jhonson, P. B., and R.W. Christy. (1972)." Optical Constants of the Noble Metals." Physical Review Letters, 6(12).